

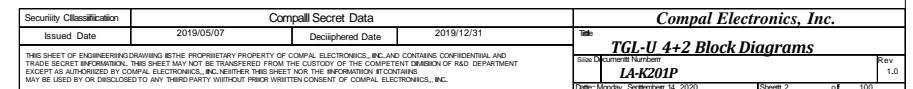
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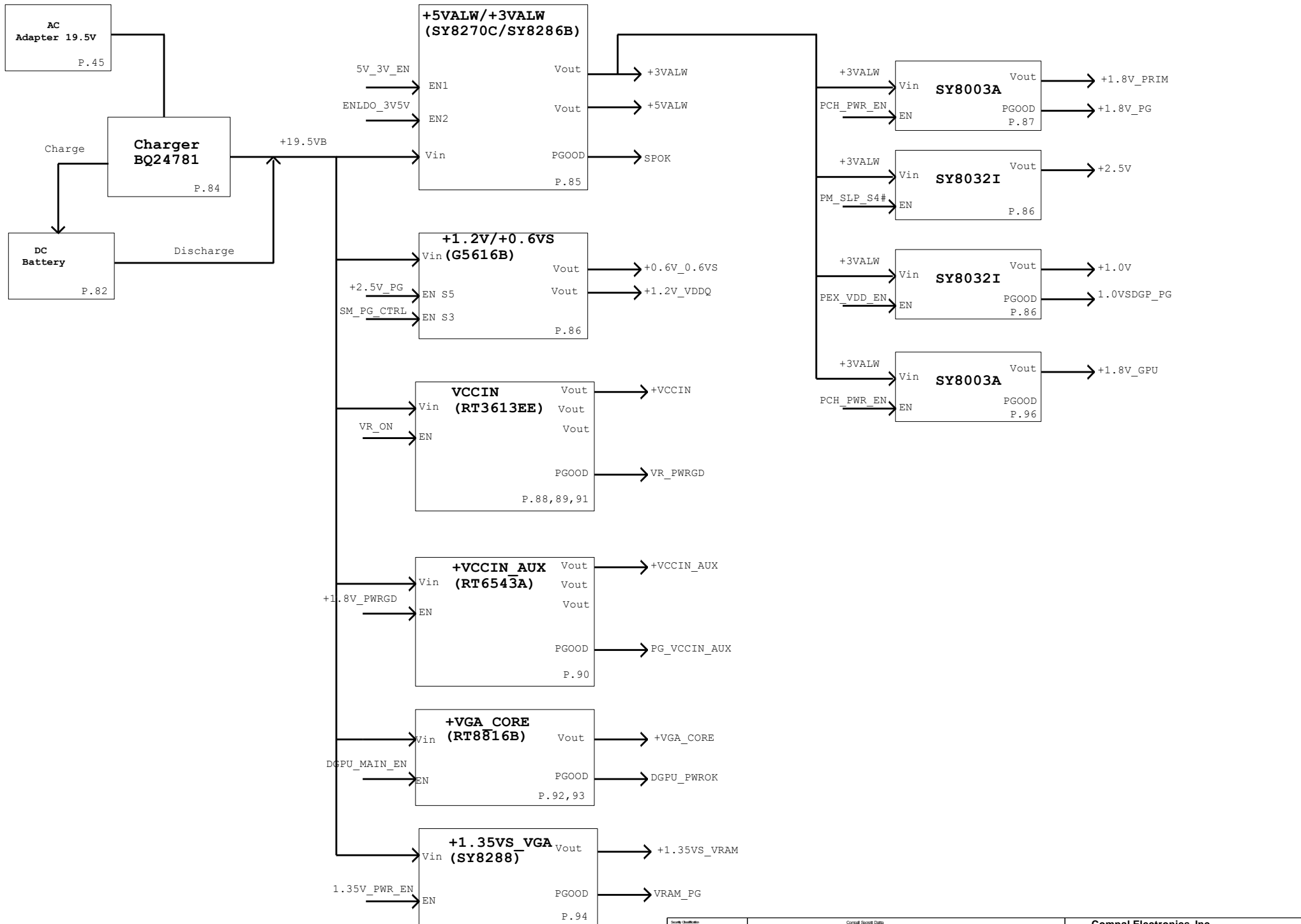
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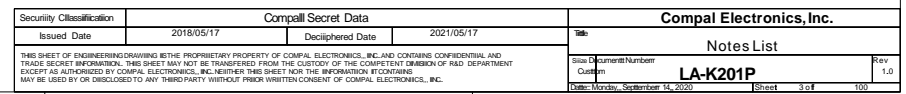
LA-K201P

2020-09-18 REV 1.0

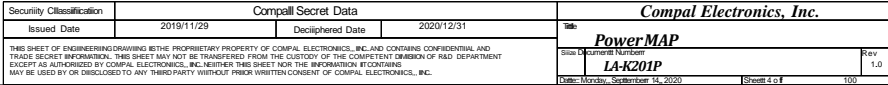
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				Size	Document Number
				Rev	1.0
Date:		Monday, September 14, 2020		Sheet	1 of 100







FQA01 Schematic: LA-H891PR01_0401A

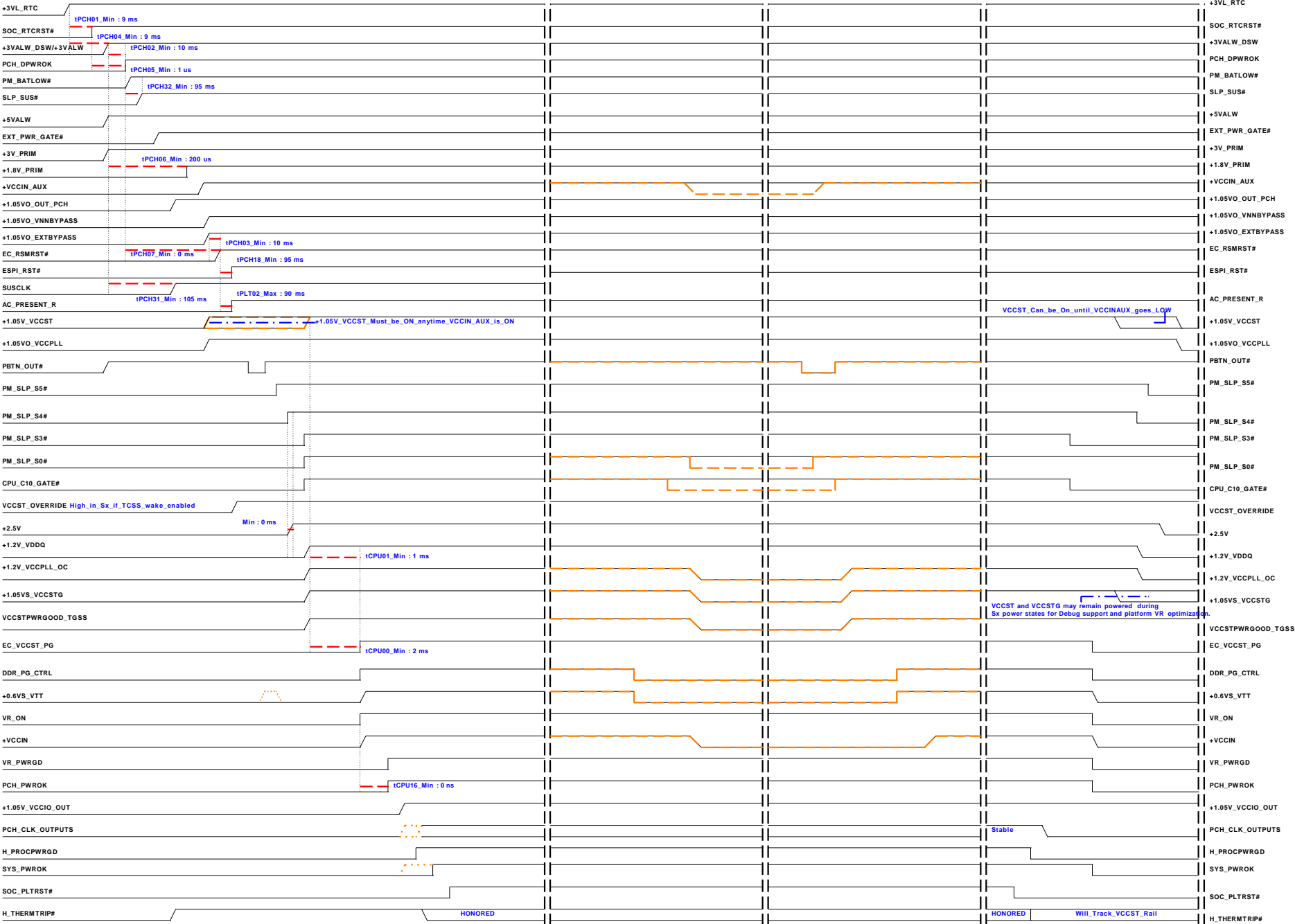


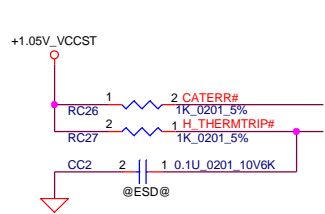
G3->S0

S0-> S0iX

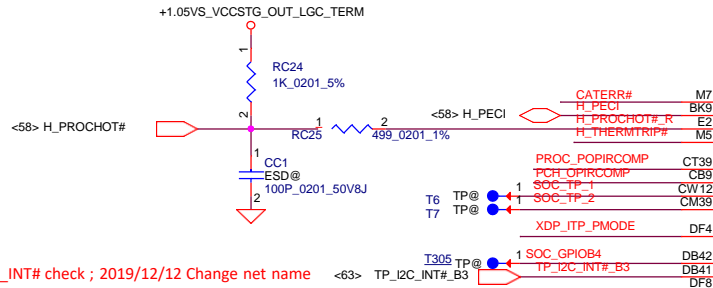
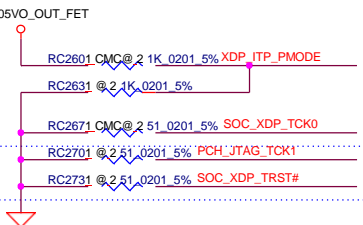
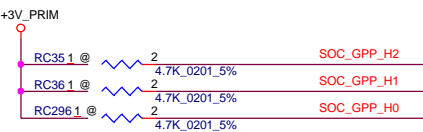
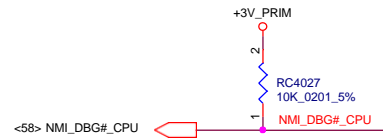
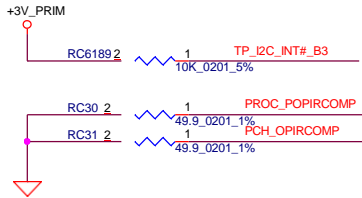
S0iX ->S0

S0->S5

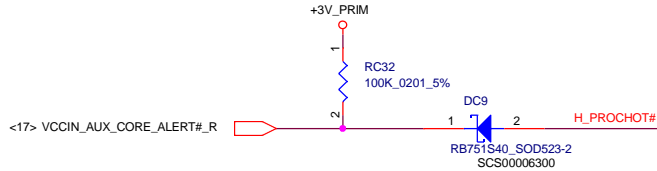




12/9 Remove XDP_SPI_SI @ PH



EC_SLP_S0IX# on Page 9

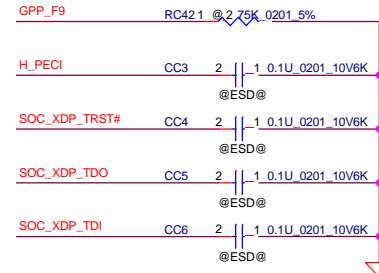
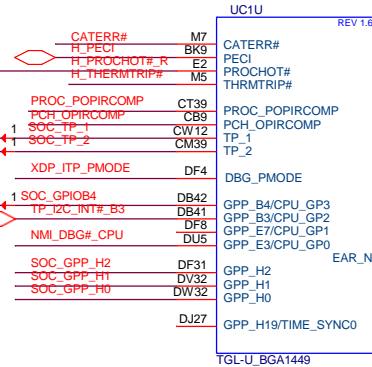
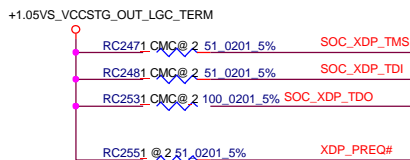


SOC_GPP_H2
BOOT STRAP3 - BIT3
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

SOC_GPP_H1
BOOT STRAP1 - BIT2
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

SOC_GPP_H0
BOOT STRAP1 - BIT1
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

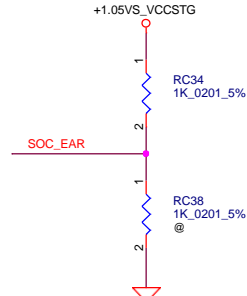
XDP_ITP_PMODE
DFX TEST MODE
INTERNAL PU 20K
This strap should sample high. There should NOT be any on-board device driving it to opposite direction during strap sampling.



SOC_WWAN_WAKE#-->GPP_F7
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direct i on during strap sampling.
INTERNALPD 20K



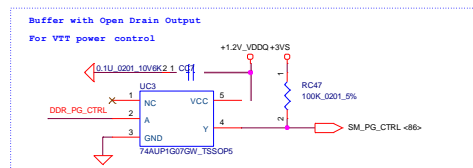
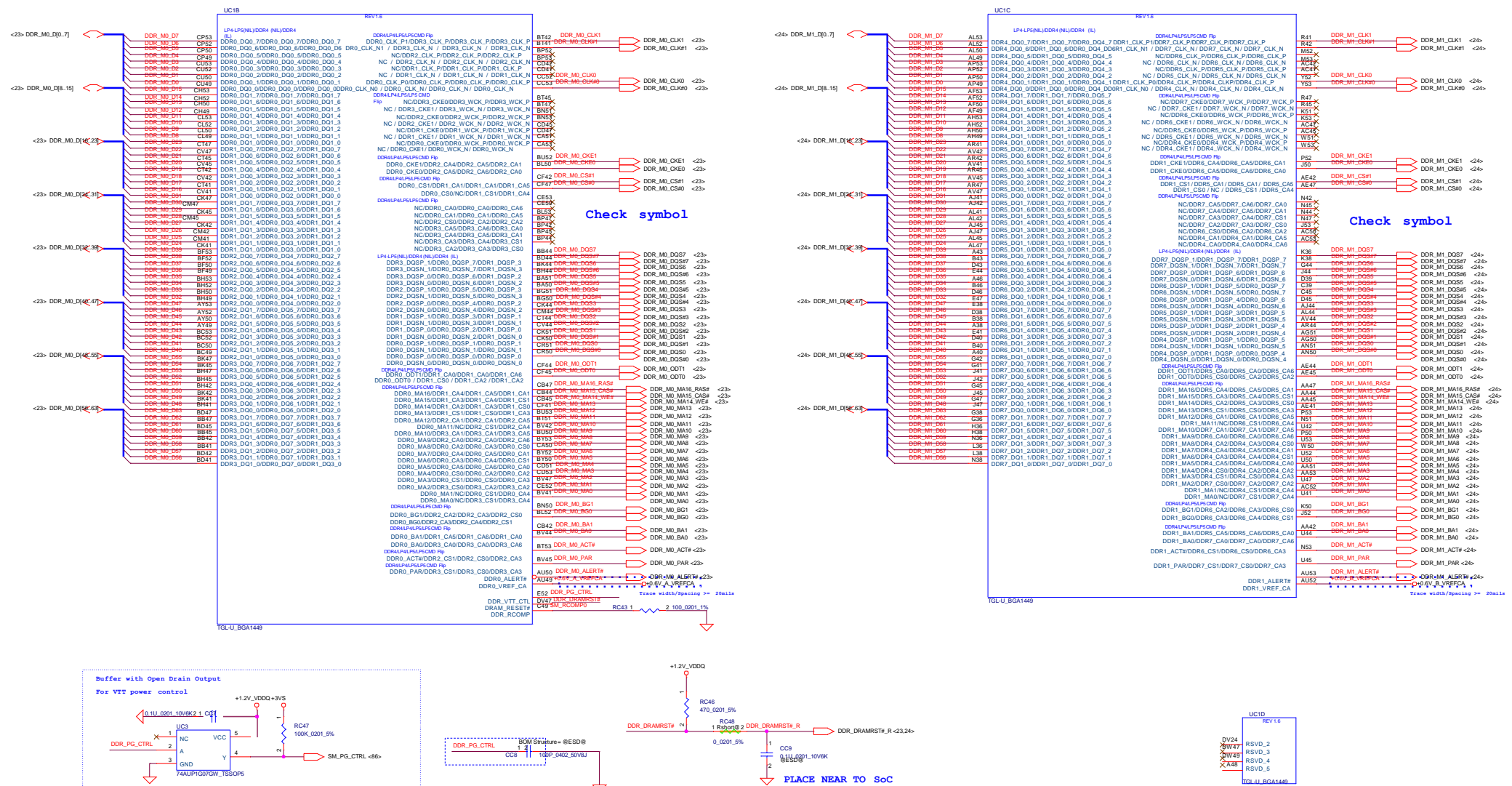
SOC_WWAN_RST#-->GPP_F10
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direct i on during strap sampling.
INTERNALPD 20K



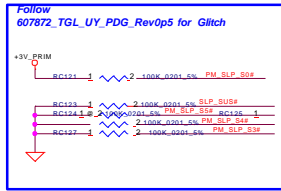
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								TGL-UP3(1/14)DDI,MSIC,XDP	
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Follow Intel DDR4 NIL

DDR4: Refer to 609003_TGL_U_DDR4_SODIMM_RVP_SCH_REV0p5



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Date: 2020/06/23				Drawn: 8-2	Rev: 1.2



SSD
WLAN
LAN
dGPU

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<52> CLK_PCIE_P2
<52> CLK_PCIE_N2
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CLK_PCIE_N3
CLK_PCIE_P2
CLK_PCIE_N2
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CLK_PCIE_N1
CLK_PEG_P0
CLK_PEG_N0

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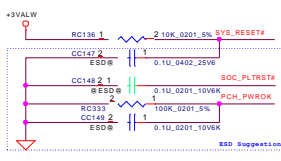
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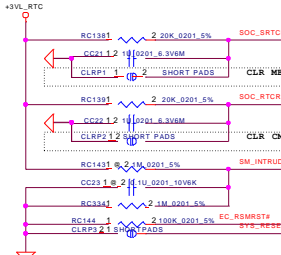
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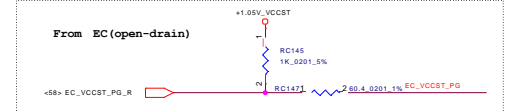
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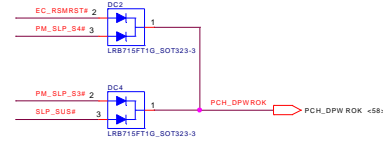
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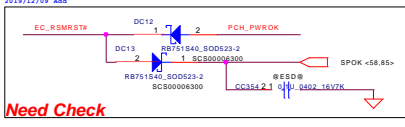
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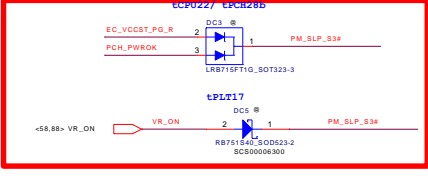
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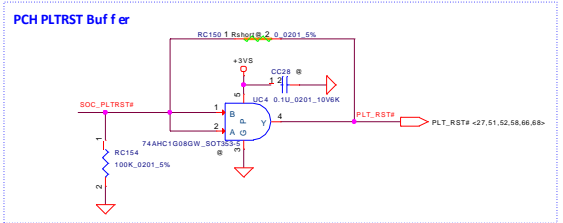
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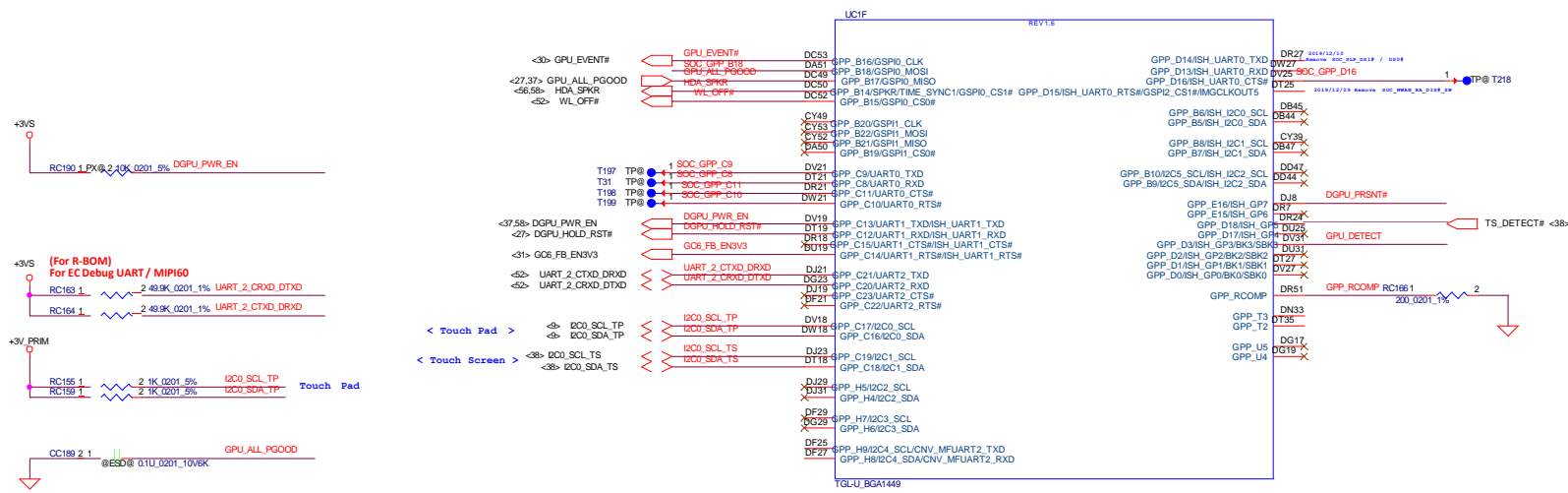
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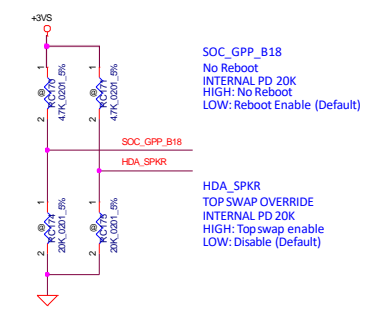
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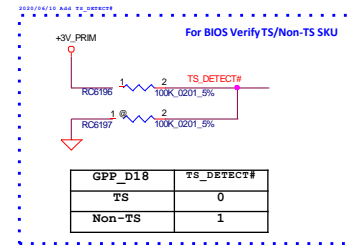
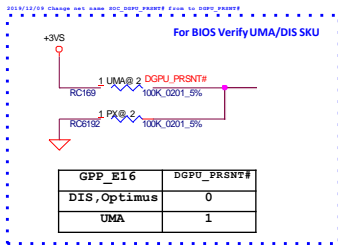
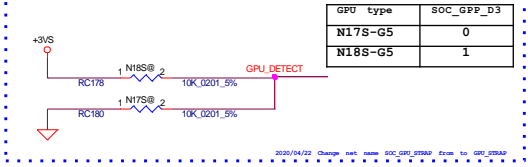
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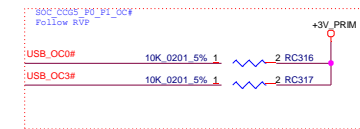
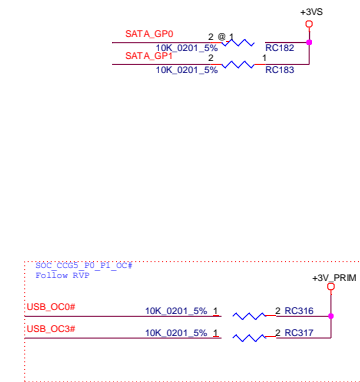


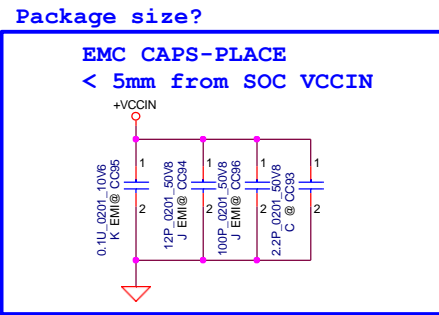
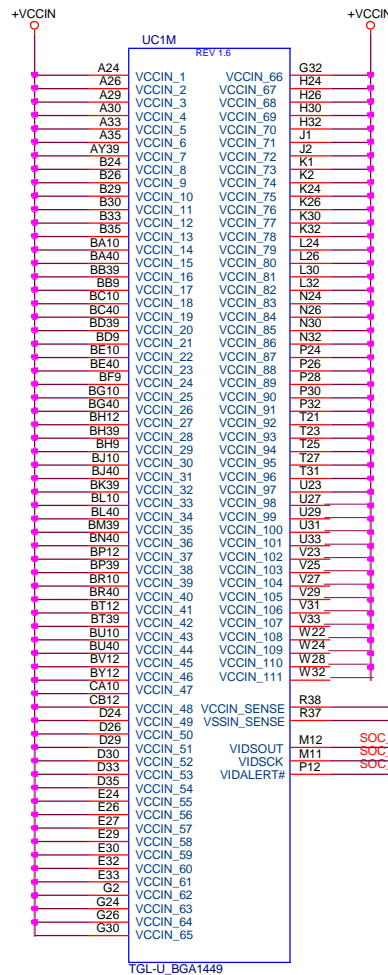
Strap Pin



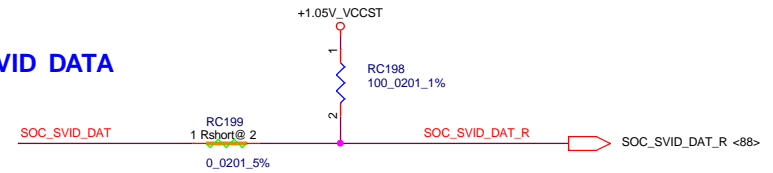
GPU Strap Pin



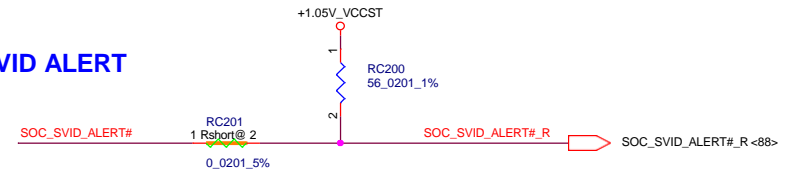




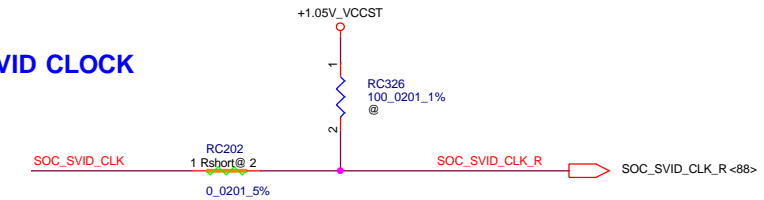
SVID DATA



SVID ALERT

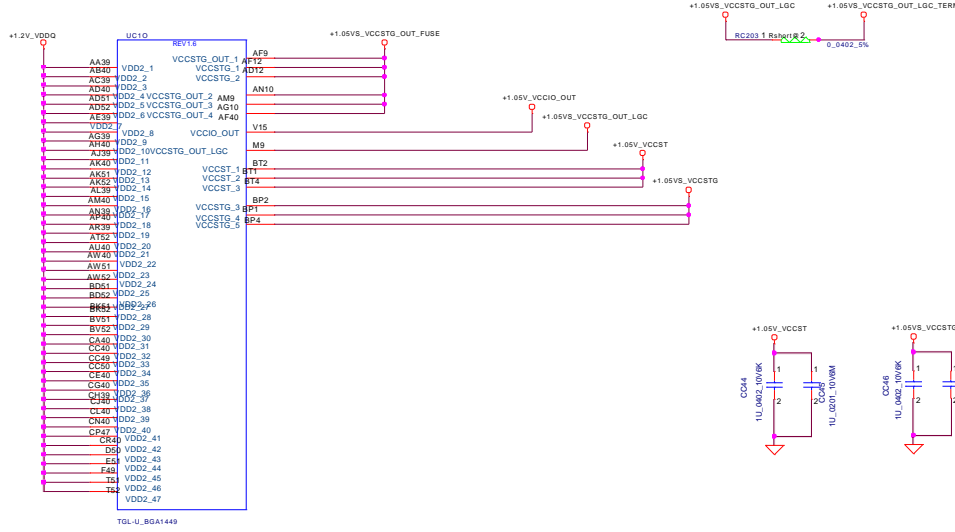
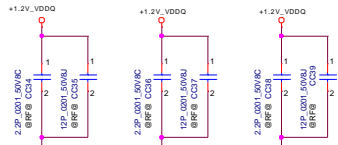


SVID CLOCK

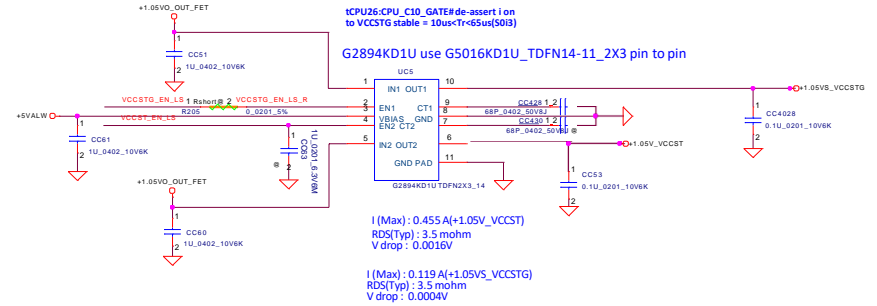


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				Date	Monday, September 14, 2020
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EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMI@)
2.2pF* 3 (EMI@)



12/23 VCCST/VCCSTG change to dual load switch



Place on CPU Side
1uF* 10
10uF* 16
47uF * 2

Figure 228. VCCST Enable Logic

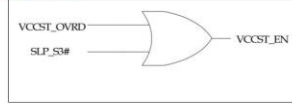
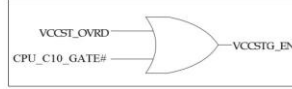
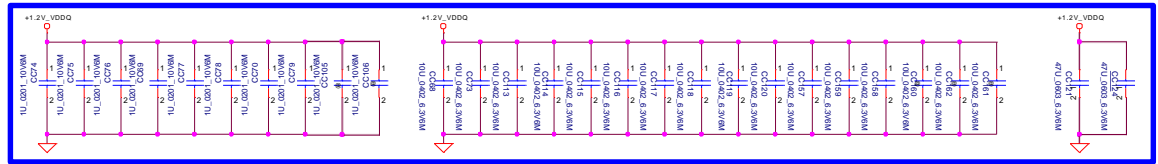
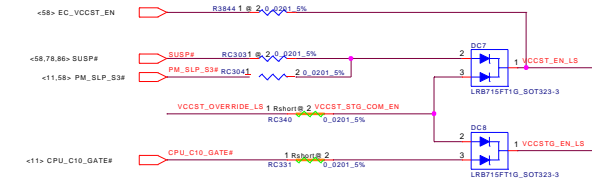
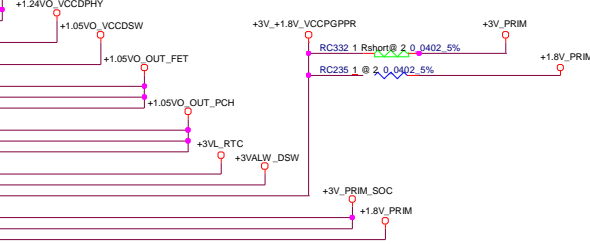
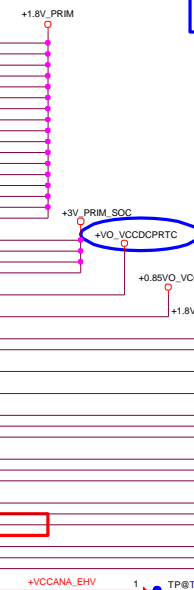
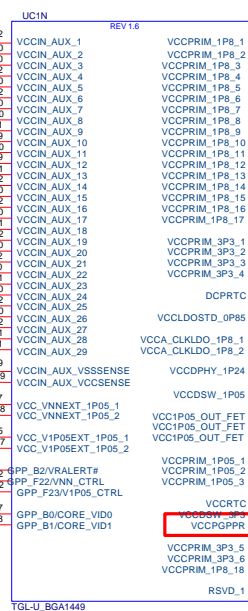
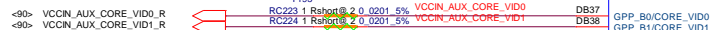
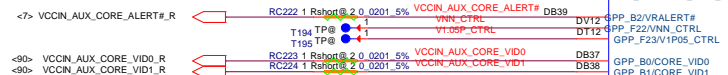
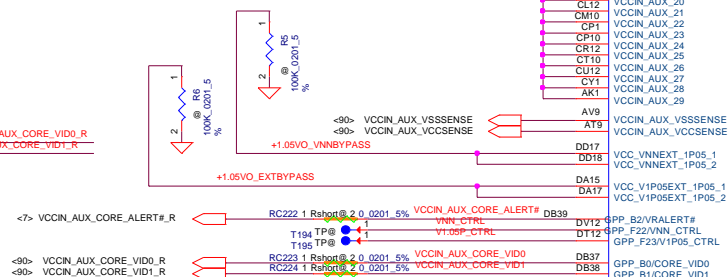
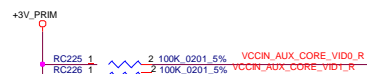
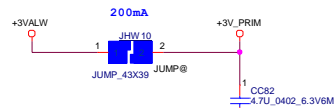
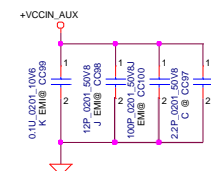
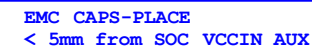
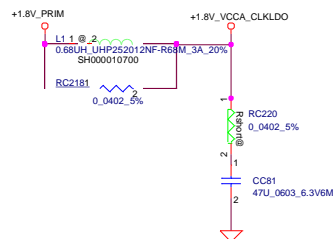
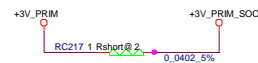


Figure 229. VCCSTG Enable Logic



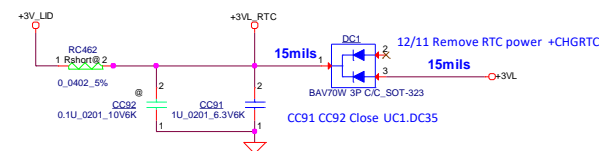
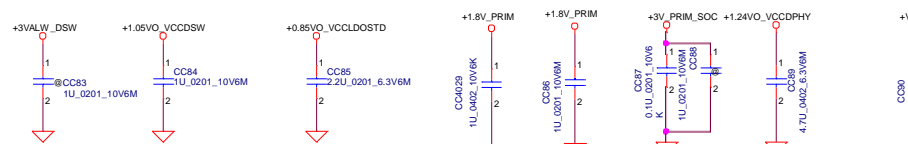
VCCST/VCCSTG Enable





NOTE:
576591-tgl-pch-lp-eds-vollof2-rev0p5
VCCPGPPR: Audio Power 3.5V, 1.8V, or 1.5V
Need to sync with codec VDDIO.

607872_TGL_UY_PDG_Rev0p5
When configured as 3.3V or 1.8V, VCCPGPPR can be merged directly with either
VCCPRIM IP8 or VCCPRIM 3P3 depending on their operating voltage.



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				Size/Document Number	Rev
				LA-K201P	1.0
Date: Monday, September 14, 2020				Sheet	17 of 100

Follow
609003_TGL_U_DDR4_SODIMM_RVP_SCH_REV0p5

T85 TP@ 1

UC1P

REV 1.6

A27	VSS_223	VSS_289	B19
A32	VSS_224	VSS_290	B2
A45	VSS_225	VSS_291	B23
A49	VSS_226	VSS_292	B27
AA41	VSS_227	VSS_293	B32
AA48	VSS_228	VSS_294	B36
AB5	VSS_229	VSS_295	B39
AB7	VSS_230	VSS_296	B42
AB8	VSS_231	VSS_297	B48
AC44	VSS_232	VSS_298	B52
AC49	VSS_233	VSS_299	B8
AD4	VSS_234	VSS_300	BA48
AD48	VSS_235	VSS_301	BA53
AD8	VSS_236	VSS_302	BB4
AF4	VSS_237	VSS_303	BB8
AG41	VSS_238	VSS_304	BC2
AG42	VSS_239	VSS_305	BD12
AG44	VSS_240	VSS_306	BD4
AG45	VSS_241	VSS_307	BD48
AG47	VSS_242	VSS_308	BD6
AG48	VSS_243	VSS_309	BF39
AG53	VSS_244	VSS_310	BF4
AH4	VSS_245	VSS_311	BF41
AH8	VSS_246	VSS_312	BF42
AK12	VSS_247	VSS_313	BF44
AK4	VSS_248	VSS_314	BF45
AK48	VSS_249	VSS_315	BF47
AK5	VSS_250	VSS_316	BF5
AK7	VSS_251	VSS_317	BF7
AK7	VSS_252	VSS_318	BF7
AK8	VSS_253	VSS_319	BF8
AM1	VSS_254	VSS_320	BG48
AM2	VSS_255	VSS_321	BG53
AM4	VSS_256	VSS_322	BH1
AM8	VSS_257	VSS_323	BH2
AN41	VSS_258	VSS_324	BH4
AN42	VSS_259	VSS_325	BH8
AN44	VSS_260	VSS_326	BK12
AN45	VSS_261	VSS_327	BK4
AN47	VSS_262	VSS_328	BK48
AN48	VSS_263	VSS_329	BK8
AN53	VSS_264	VSS_330	BL49
AP4	VSS_265	VSS_331	BM1
AP8	VSS_266	VSS_332	BM4
AT4	VSS_267	VSS_333	BM41
AT48	VSS_268	VSS_334	BM42
AT51	VSS_269	VSS_335	BM44
AT5	VSS_270	VSS_336	BM45
AV12	VSS_271	VSS_337	BM47
AV39	VSS_272	VSS_338	BM8
AV4	VSS_273	VSS_339	BN48
AV5	VSS_274	VSS_340	BP41
AV7	VSS_275	VSS_341	BP49
AV8	VSS_276	VSS_342	BP5
AW1	VSS_277	VSS_343	BP50
AW2	VSS_278	VSS_344	BP7
AW48	VSS_279	VSS_345	BT44
AY4	VSS_280	VSS_346	BT48
AY41	VSS_281	VSS_347	BU49
AY42	VSS_282	VSS_348	BV3
AY44	VSS_283	VSS_349	BV48
AY45	VSS_284	VSS_350	BV5
AY47	VSS_285	VSS_351	BW10
AY8	VSS_286	VSS_352	BY41
AY9	VSS_287	VSS_353	BY42
B13	VSS_288		

TGL-U_BGA1449

UC1Q

REV 1.6

BY44	VSS_109	VSS_169	CY44
BY45	VSS_110	VSS_170	CY47
BY47	VSS_111	VSS_171	CY5
BY49	VSS_112	VSS_172	D27
C13	VSS_113	VSS_173	D32
C19	VSS_114	VSS_174	D36
C23	VSS_115	VSS_175	D42
CA48	VSS_116	VSS_176	D49
CB41	VSS_117	VSS_177	D5
CC10	VSS_118	VSS_178	DA30
CC3	VSS_119	VSS_179	DA33
CC5	VSS_120	VSS_180	DA53
CD44	VSS_121	VSS_181	DC17
CD48	VSS_122	VSS_182	DD15
CD7	VSS_123	VSS_183	DD24
CE49	VSS_124	VSS_184	DD26
CG48	VSS_125	VSS_185	DD28
CG51	VSS_126	VSS_186	DD31
CG52	VSS_127	VSS_187	DD33
CG9	VSS_128	VSS_188	DD35
CH41	VSS_129	VSS_189	DD39
CH42	VSS_130	VSS_190	DD45
CH44	VSS_131	VSS_191	DE5
CH45	VSS_132	VSS_192	DD51
CH47	VSS_133	VSS_193	DD52
CJ3	VSS_134	VSS_194	DE3
CJ5	VSS_135	VSS_195	DE5
CJ9	VSS_136	VSS_196	DF19
CK39	VSS_137	VSS_197	DG15
CK48	VSS_138	VSS_198	DG21
CK53	VSS_139	VSS_199	DG27
CL9	VSS_140	VSS_200	DG33
CL12	VSS_141	VSS_201	DG39
CL48	VSS_142	VSS_202	DG45
CN48	VSS_143	VSS_203	DG5
CN51	VSS_144	VSS_204	DG5
CN52	VSS_145	VSS_205	DG53
CN9	VSS_146	VSS_206	DG6
CP3	VSS_147	VSS_207	DJ1
CP41	VSS_148	VSS_208	DJ2
CP42	VSS_149	VSS_209	DJ4
CP44	VSS_150	VSS_210	DK51
CP45	VSS_151	VSS_211	DL3
CP5	VSS_152	VSS_212	DL5
CR48	VSS_153	VSS_213	DM10
CR53	VSS_154	VSS_214	DM15
CR9	VSS_155	VSS_215	DM21
CT5	VSS_156	VSS_216	DM27
CU4	VSS_157	VSS_217	DM33
CU9	VSS_158	VSS_218	DM39
CV10	VSS_159	VSS_219	DM4
CV48	VSS_160	VSS_220	DM45
CV5	VSS_161	VSS_221	DN1
CV51	VSS_162	VSS_222	DN2
CV52	VSS_163		
CY17	VSS_164		
CY22	VSS_165		
CY35	VSS_166		
CY41	VSS_167		
CY42	VSS_168		

TGL-U_BGA1449

UC1R

REV 1.6

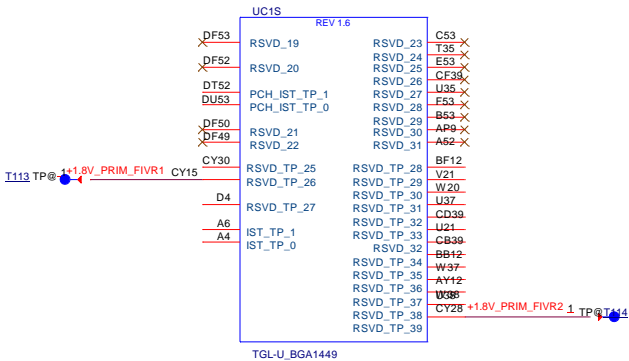
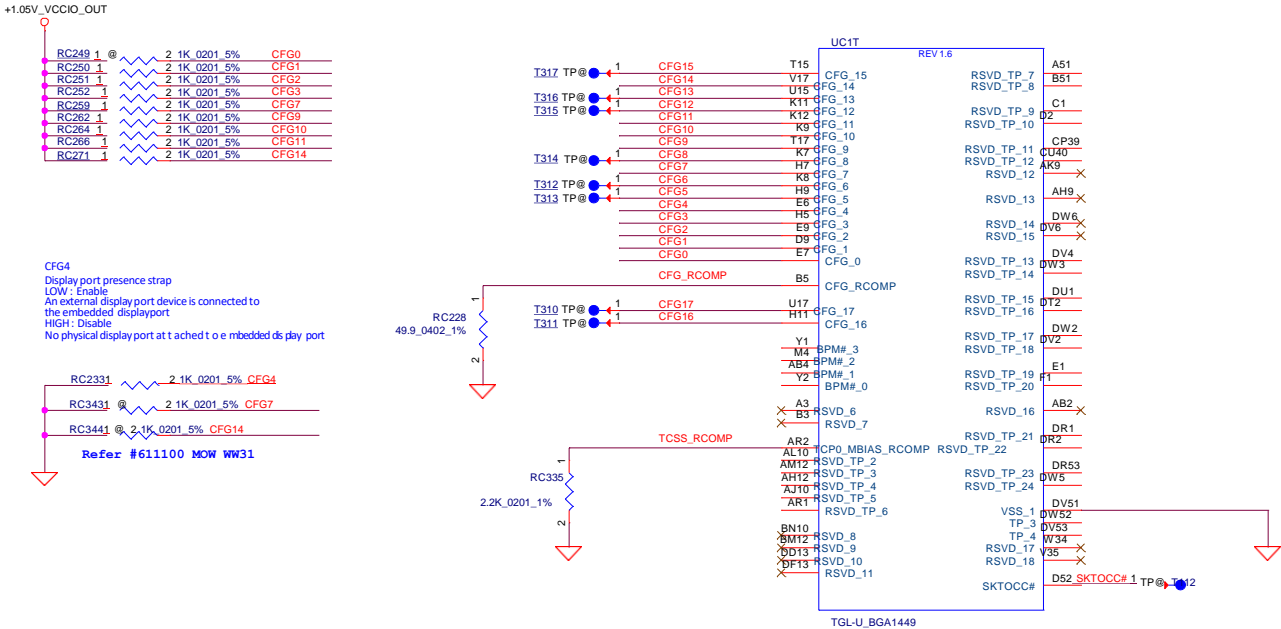
DP53	VSS_2	VSS_46	K34
DR11	VSS_3	VSS_47	K49
DR16	VSS_4	VSS_48	K5
DR22	VSS_5	VSS_49	L22
DR28	VSS_6	VSS_50	L28
DR34	VSS_7	VSS_51	L34
DR40	VSS_8	VSS_52	L39
DR46	VSS_9	VSS_53	L41
DT4	VSS_10	VSS_54	L42
DT50	VSS_11	VSS_55	L44
DU11	VSS_12	VSS_56	L45
DU16	VSS_13	VSS_57	L47
DU22	VSS_14	VSS_58	L49
DU28	VSS_15	VSS_59	M1
DU34	VSS_16	VSS_60	M2
DU40	VSS_17	VSS_61	M50
DU46	VSS_18	VSS_62	N22
DV1	VSS_19	VSS_63	N28
DV40	VSS_20	VSS_64	N34
DV52	VSS_21	VSS_65	N39
DW51	VSS_22	VSS_66	N41
E13	VSS_23	VSS_67	N48
E19	VSS_24	VSS_68	P11
E35	VSS_25	VSS_69	P14
E48	VSS_26	VSS_70	P16
G22	VSS_27	VSS_71	P18
G28	VSS_28	VSS_72	P20
G34	VSS_29	VSS_73	P22
G39	VSS_30	VSS_74	P33
G48	VSS_31	VSS_75	P35
G51	VSS_32	VSS_76	P4
G52	VSS_33	VSS_77	P49
H12	VSS_34	VSS_78	P8
H22	VSS_35	VSS_79	R39
H28	VSS_36	VSS_80	R44
H34	VSS_37	VSS_81	T19
H8	VSS_38	VSS_82	T29
J39	VSS_39	VSS_83	T33
J49	VSS_40	VSS_84	T4
K16	VSS_41	VSS_85	T48
K18	VSS_42	VSS_86	T5
K20	VSS_43	VSS_87	U19
K22	VSS_44	VSS_88	U25
K28	VSS_45	VSS_89	U39
		VSS_90	U49
		VSS_91	V19
		VSS_92	V4
		VSS_93	V8
		VSS_94	W16
		VSS_95	W19
		VSS_96	W26
		VSS_97	W30
		VSS_98	W39
		VSS_99	W41
		VSS_100	W42
		VSS_101	W44
		VSS_102	W45
		VSS_103	W47
		VSS_104	W48
		VSS_105	Y4
		VSS_106	Y49
		VSS_107	Y50
		VSS_108	Y8

TGL-U_BGA1449

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				Date	Monday, September 14, 2020
				Sheet	18 of 100
				Rev	1.0

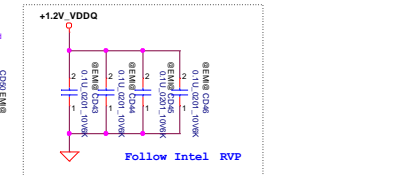
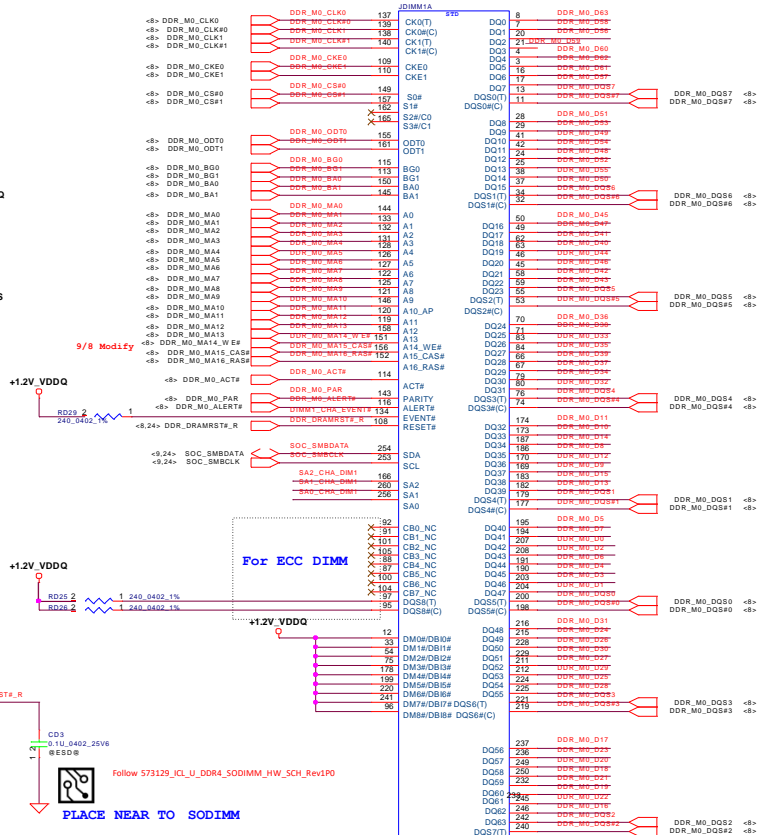
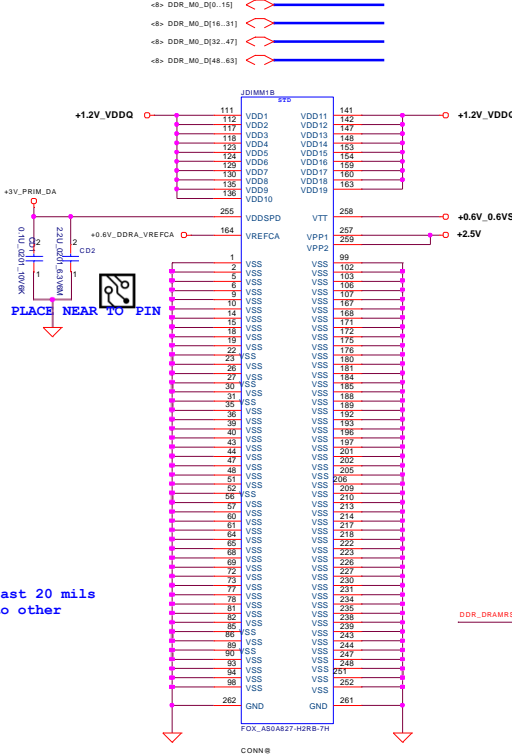
CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

Processor BPM#[3:0] nets can be left floated when not use for debug. Processor CFGI19:01 and PCH chipset test interfaces might have dual purpose usage. From

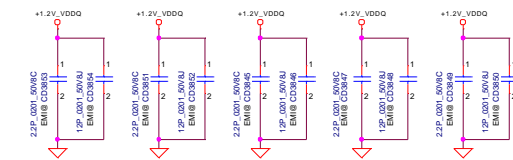


REVERSE TYPE

Non-Interleaved Memory



EMC CAPS-PLACE
< 4mm from SO-DIMM VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)



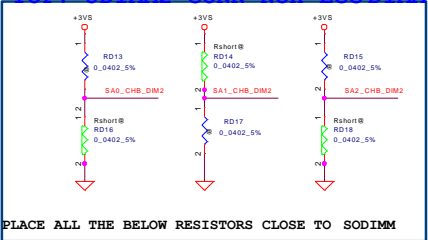
Security Classification		Compall Secret Data		Compal Electronics, Inc.	
Issued Date	2019/05/07	Declassified Date	2019/12/31	Title	
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				Rev	1.0
				Sheet	23 of 830

CHANNEL-M1

Non-Interleaved Memory

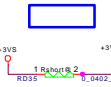
STD (5.2 mm)

TOP: JDIMM2 CONN Non-ECC DIMM



SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

12/16 Remove RD36



PLACE NEAR TO PIN



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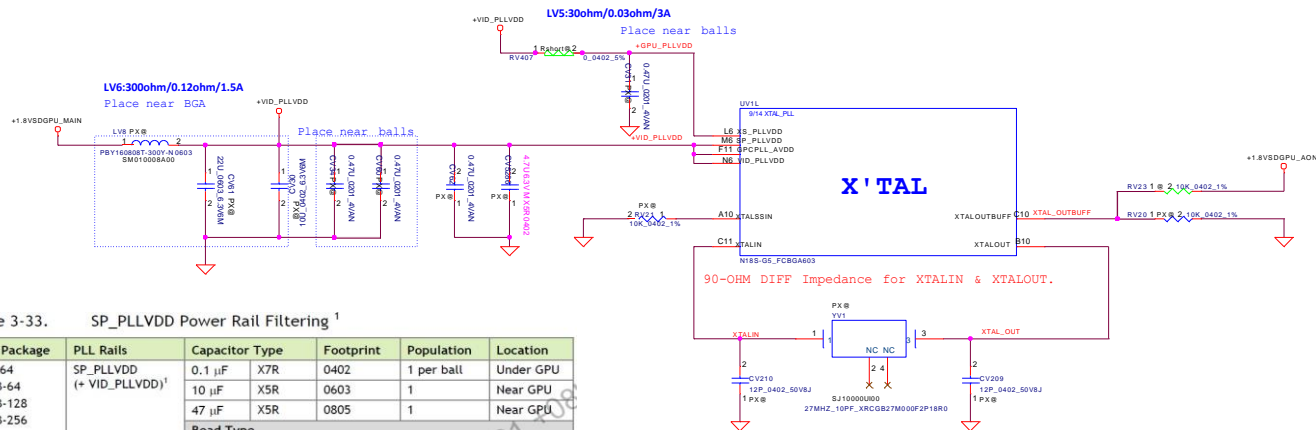
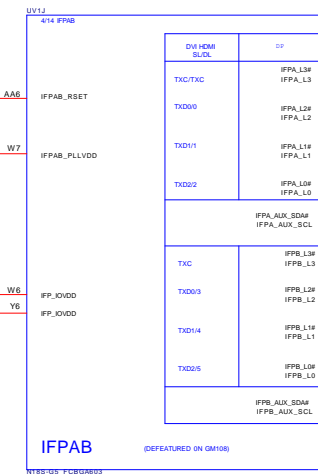
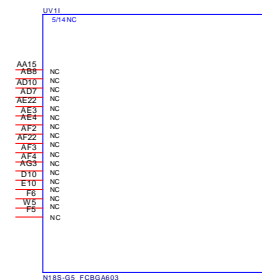
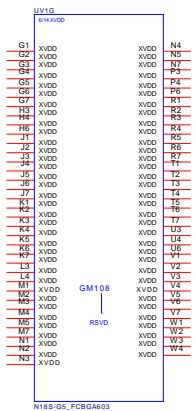
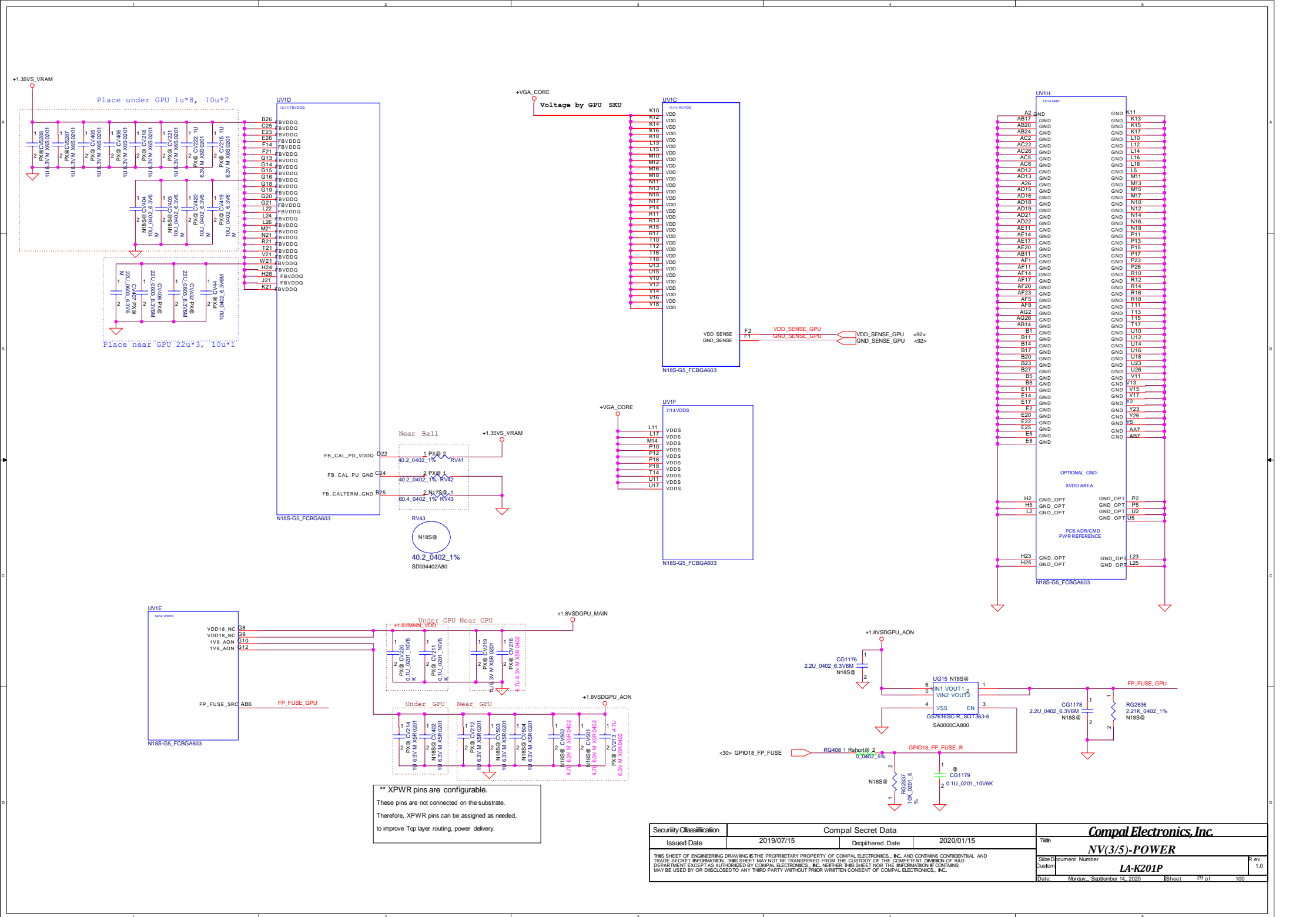
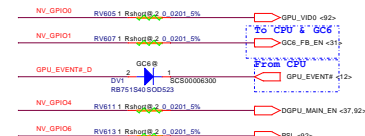
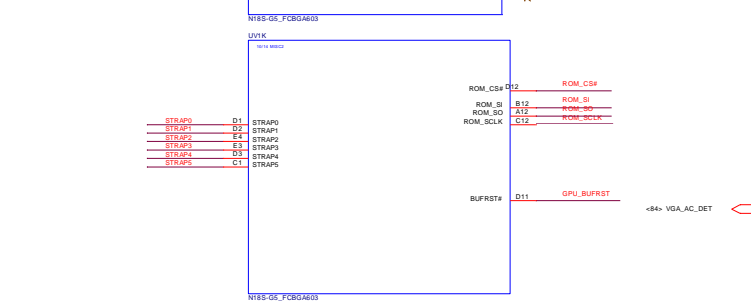


Table 3-33. SP_PLLVDD Power Rail Filtering ¹

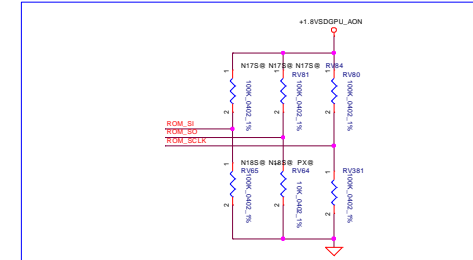
GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB2-64	SP_PLLVDD	0.1 μ F	X7R	0402	1 per ball
GB2B-64	SP_PLLVDD (+VID_PLLVDD) ¹	10 μ F	X5R	0603	1
GB4B-128		47 μ F	X5R	0805	1
GB3B-256					Near GPU
		Bead Type			
		300 Ω (ESR=0.2 Ω)	0603	1	Near GPU

Note:
1. SP_PLLVDD and VID_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.



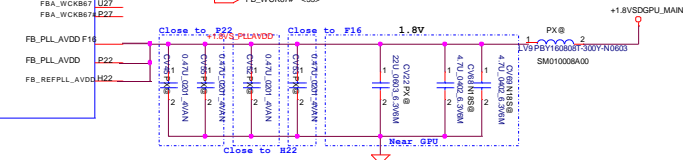
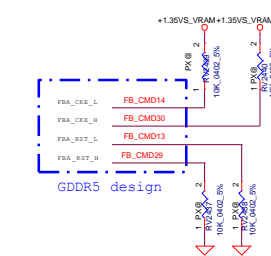
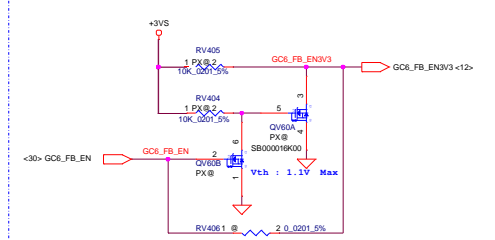
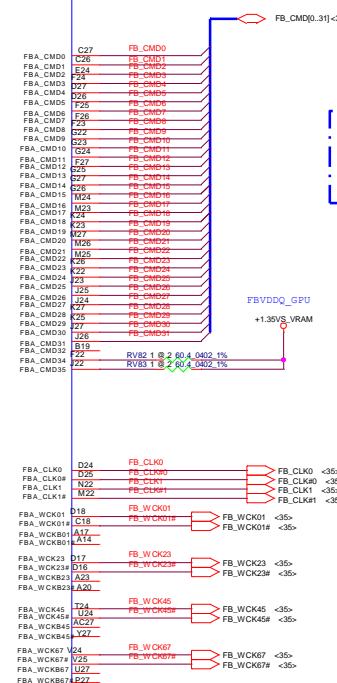
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Strap Pins <small>see Note</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001) M2G (N18S)
L	H	L	2 (0x0002) H2G (N18S)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004) S2G (N18S)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009) M2G (N17S)
L	M	H	10 (0x000A) H2G (N17S)
L	H	M	11 (0x000B) S2G (N17S)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)



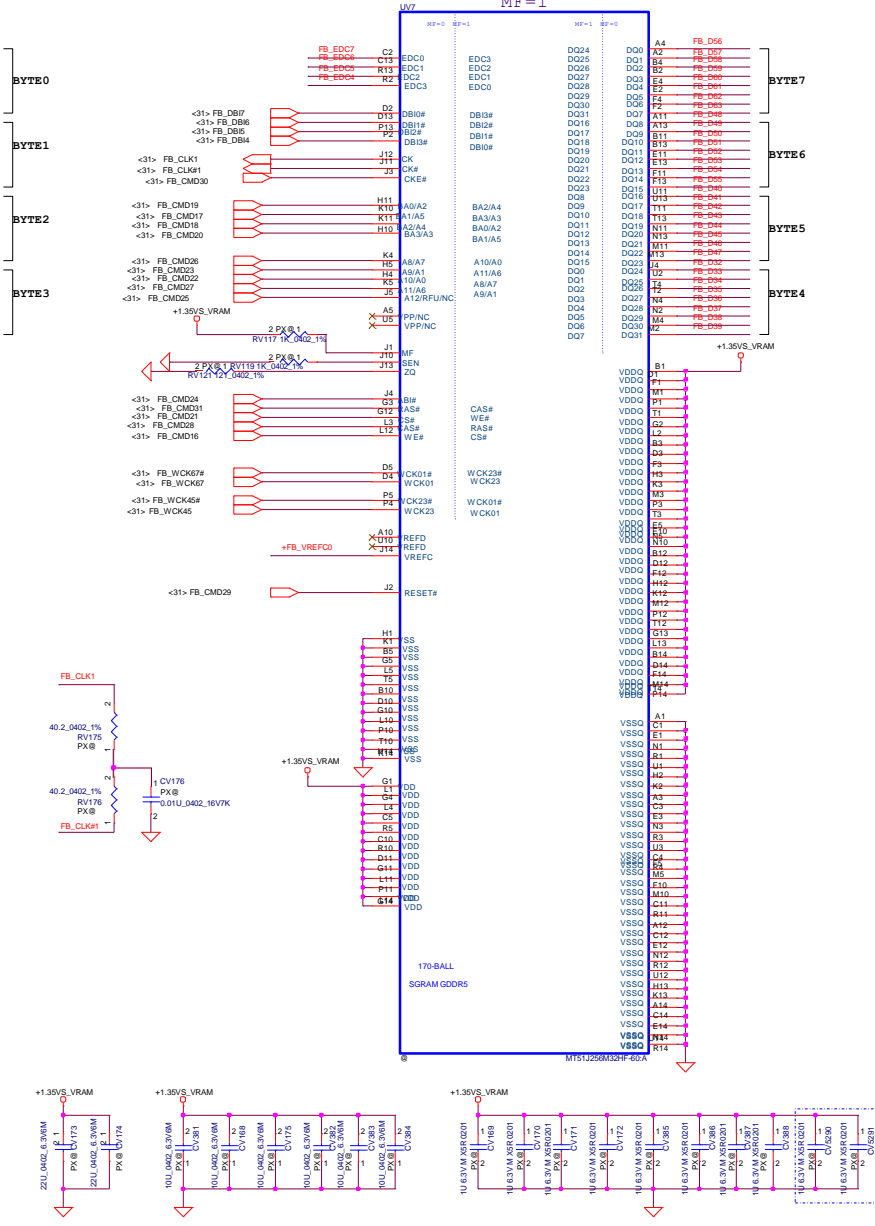
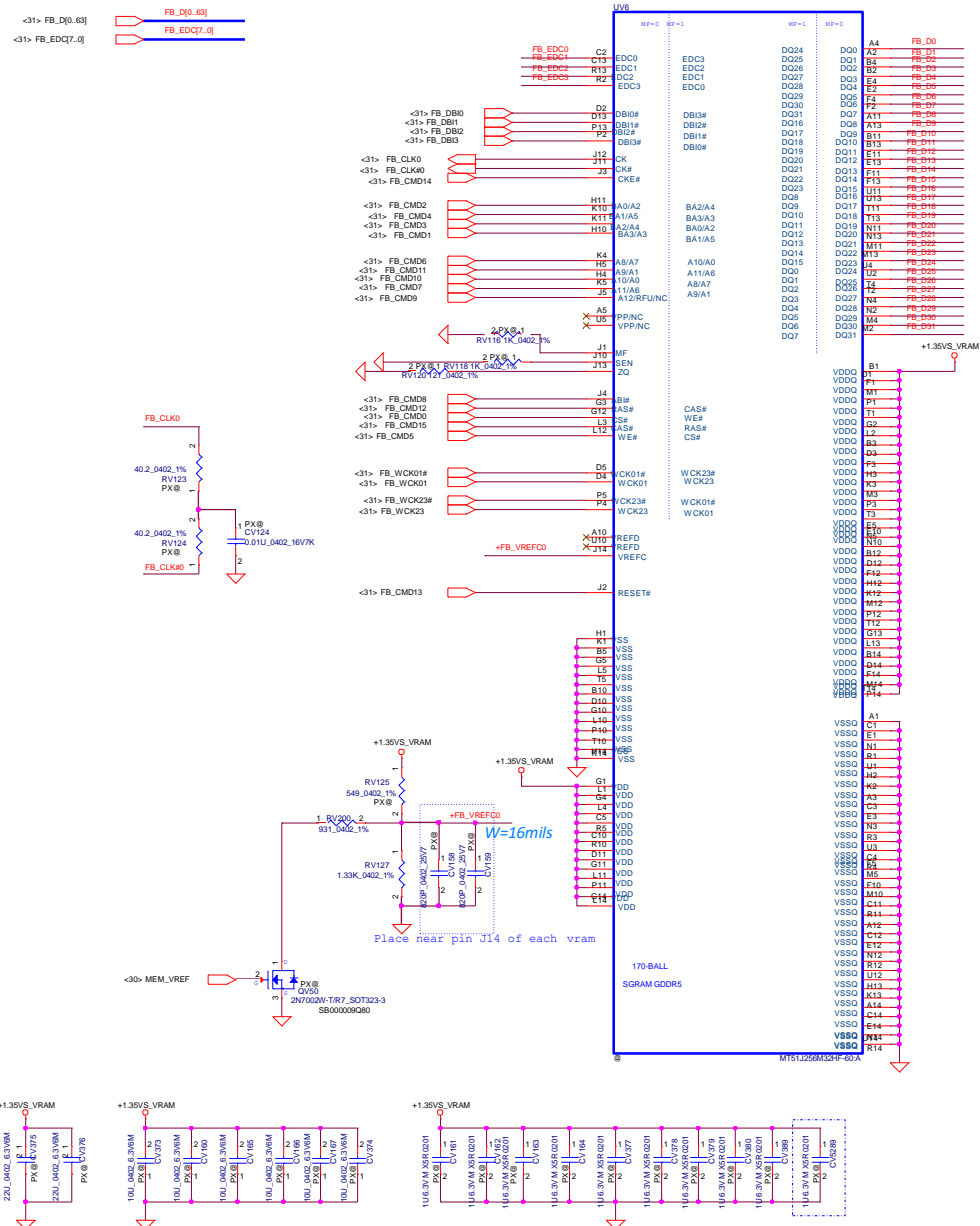
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0xB	8 Gbps	N/A	Full	Production candidate

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GCH24H-JR-ZC	A-die	0x2	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0x4	8 Gbps	N/A	Full	Production candidate

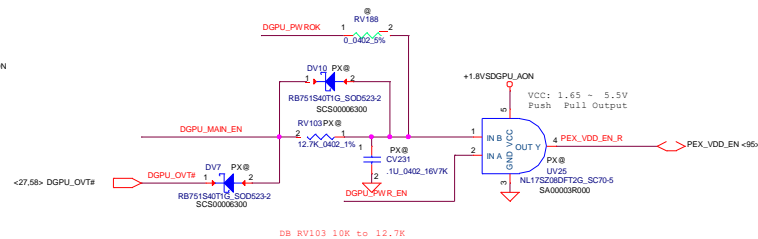


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Memory Partition A



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Timing diagram for GPU power on and off. The diagram shows four signals: PEX_RST#, GPU_PWR_EN, All Rail PGGOOD, and PCIE_Link. It illustrates two scenarios: 'GPU power off' and 'GPU power on'. In the 'GPU power off' scenario, GPU_PWR_EN transitions from high to low, and All Rail PGGOOD transitions from high to low. In the 'GPU power on' scenario, GPU_PWR_EN transitions from low to high, and All Rail PGGOOD transitions from low to high. PEX_RST# is shown as a pulse with timing T0 and T1. PCIE_Link is shown as a signal that is 'X' (unknown) during the power transition period.

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

		GPU Core	GPU FBIO	FB Total ^{1, 3}	1.05V Total ¹	3.3V Tot		
	VRAM Type	—	1.5V ⁴	1.35V ⁴	1.5V ⁴	1.35V ⁴	1.05V ⁴	3.3V ⁴
Products		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5	26.5	—	2.0	—	4.2	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Figure 3-7. Example of Power-Up Sequencing Order

The diagram shows the timing sequence for GPU Self-Refresh entry and exit. It includes signals: FB_CKE, PEX_LINK, GPU_PEX_RST#, GC6_FB_EN, 3V3_MAIN_EN, All Rail PGOOD, and GPU_EVENT#. The sequence starts with a 'GC6 Entry' phase where FB_CKE transitions from Normal to Self-Refresh, PEX_LINK transitions from Active to X, and GPU_PEX_RST# transitions from high to low. This is followed by a 'GC6 Exit' phase where FB_CKE transitions from Self-Refresh to Normal, PEX_LINK transitions from X to Detect, GPU_PEX_RST# transitions from low to high, and GPU_EVENT# transitions from low to high. The time interval between the start of the Self-Refresh phase and the start of the Detect phase is labeled T1. The time interval between the start of the Detect phase and the start of the Normal phase is labeled T0.

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	11/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

W=60mils

SM010014520 3000mA
220ohm @100mhz
DCR 0.04

VINPWR_B+

W=60mils

+10VB

0.75A 24V MF18SMF075/24
SP44000900

1 FU1

2

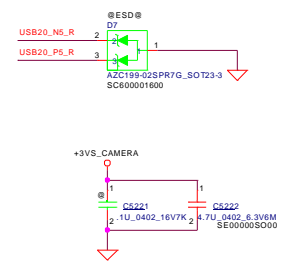
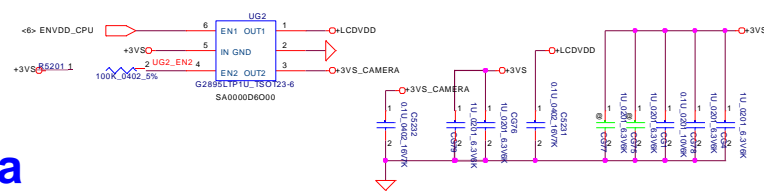
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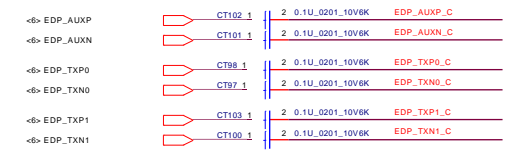
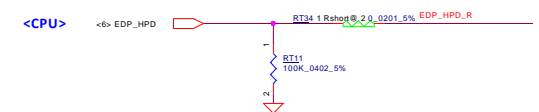
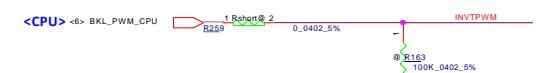
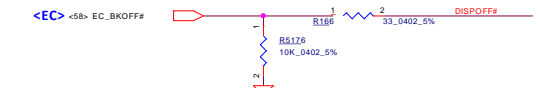
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2

GND



Touch Screen Power Selection:



Timing diagram for the ACES_31540-03001-001 SP010020L00. The diagram shows the relationship between various signals and the device's internal components.

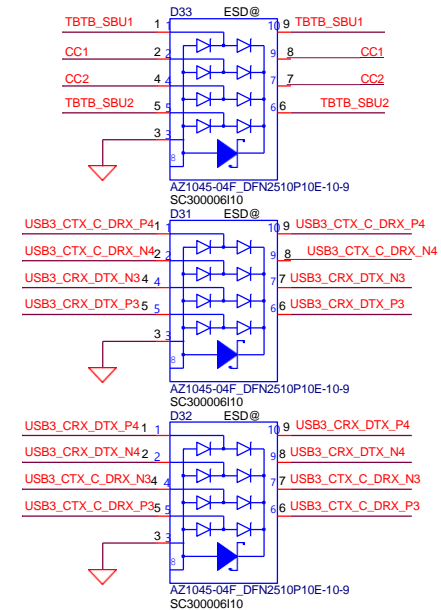
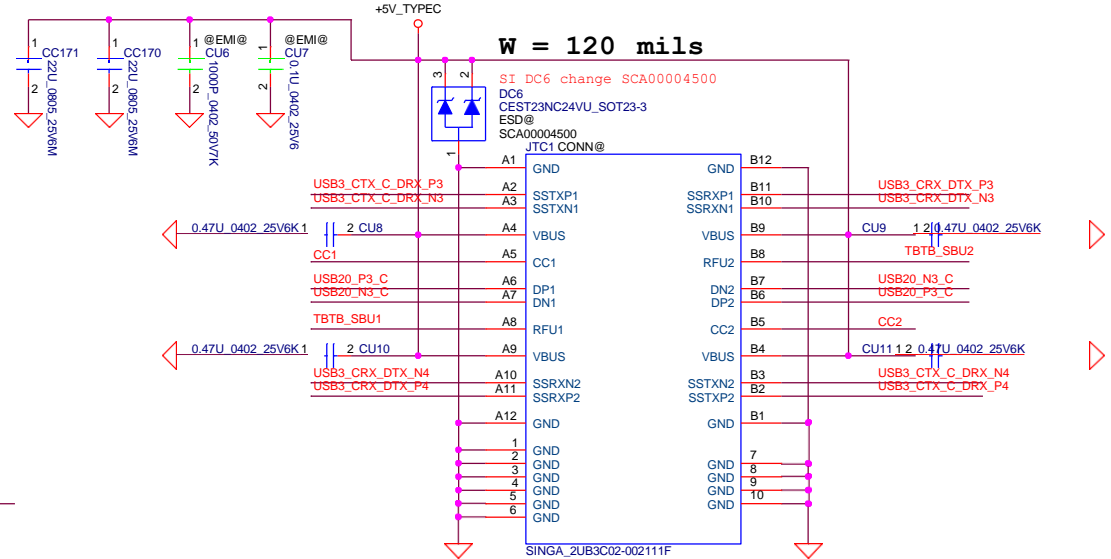
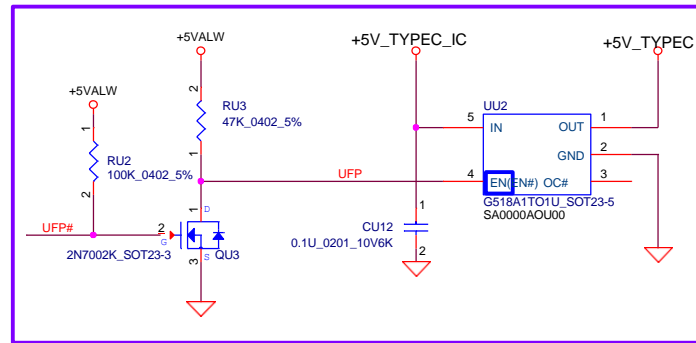
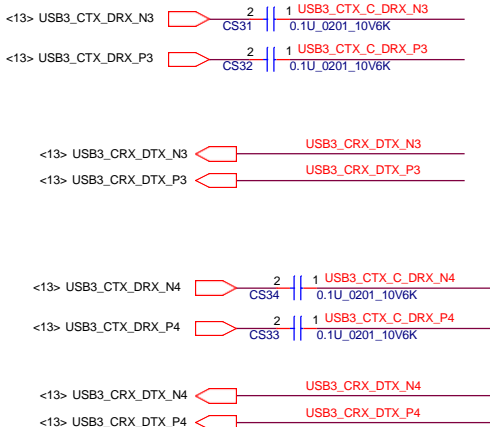
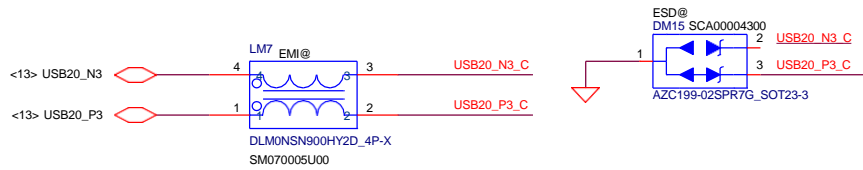
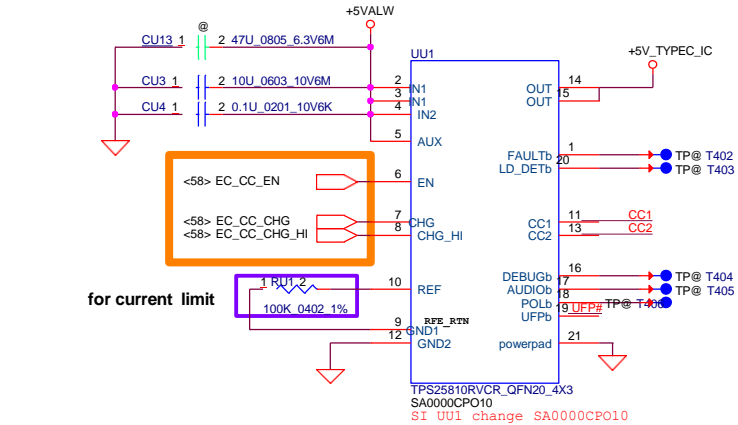
Signals and Connections:

- Touch screen:**
 - `<12> I2C0_SCL_TS` (I2C0_SCL_TS)
 - `<12> I2C0_SDA_TS` (I2C0_SDA_TS)
 - `<39> D_MIC_CLK` (D_MIC_CLK)
 - `<39> D_MIC_DATA` (D_MIC_DATA)
 - `<12> TS_DETECT#` (TS_DETECT#)
- Camera:**
 - `+3VS_TOUCH` (TS_RST#_R)
 - `+3VS_CAMERA` (USB20_HS_R, USB20_PS_R)
 - `INVPWR_B+` (INVPWR_B+)
- EDP:**
 - `EDP_TXP0_C` (EDP_TXP0_C)
 - `EDP_TXN0_C` (EDP_TXN0_C)
 - `EDP_AUXP_C` (EDP_AUXP_C)
 - `EDP_AUXN_C` (EDP_AUXN_C)
 - `EDP_HPD_R` (EDP_HPD_R)
- Other Signals:**
 - `GND1` (GND1)
 - `GND2` (GND2)

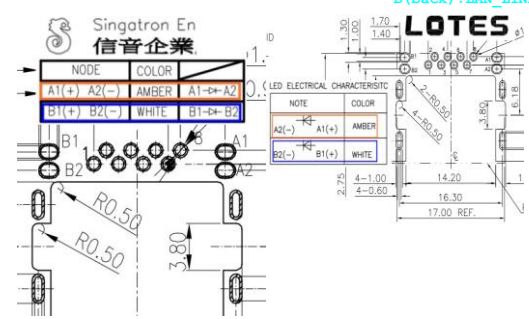
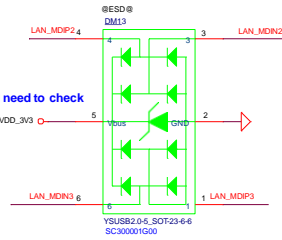
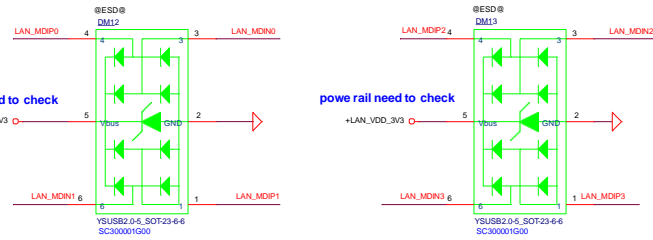
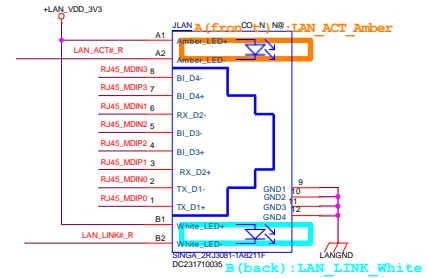
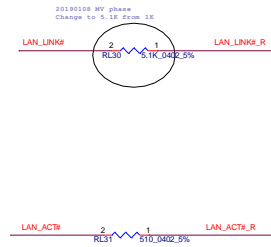
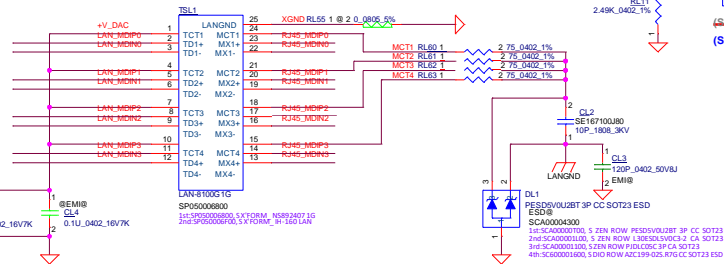
The diagram illustrates the timing and signal flow between the device and its external components, including the Touch screen, Camera, and EDP.

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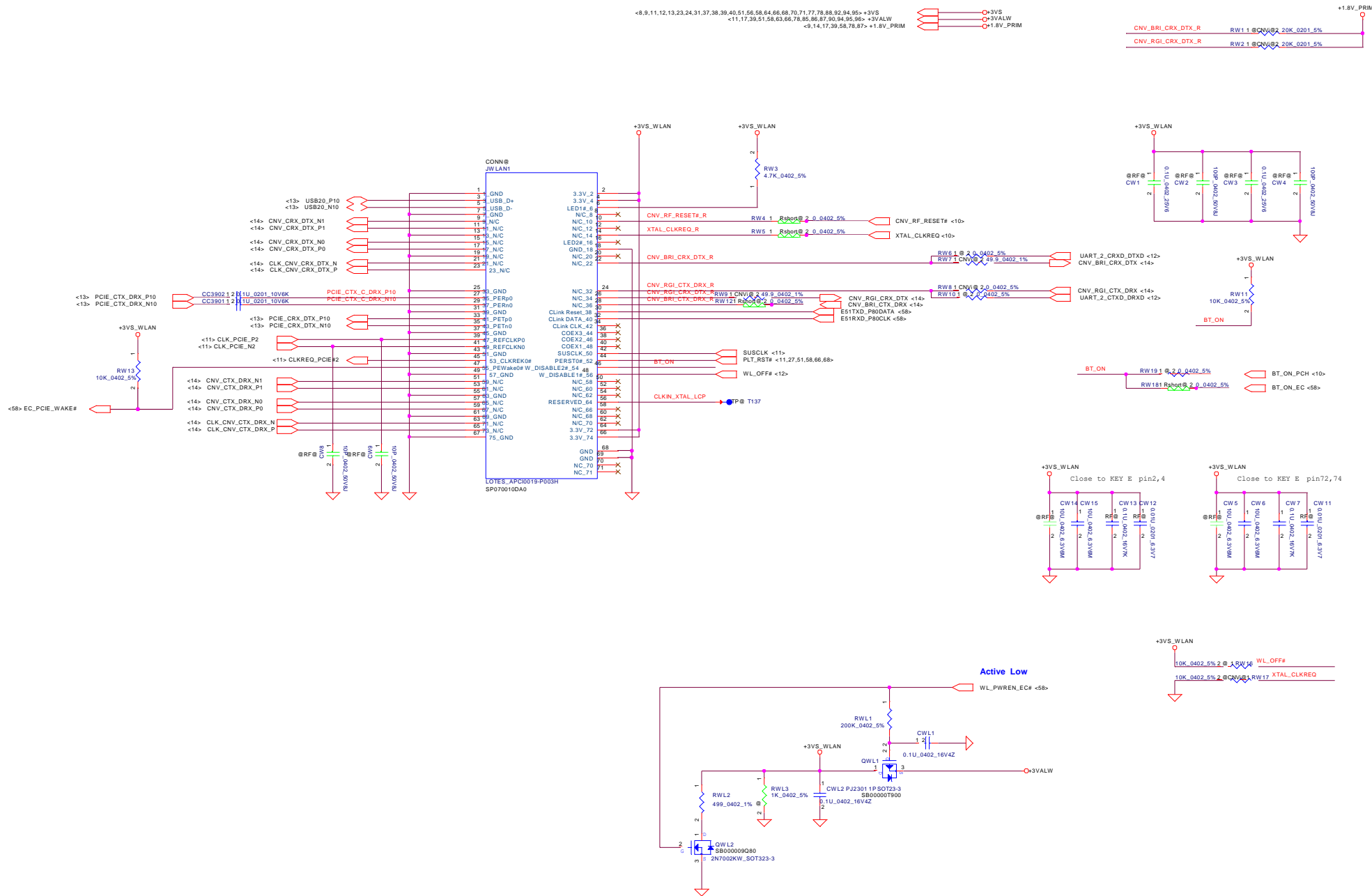
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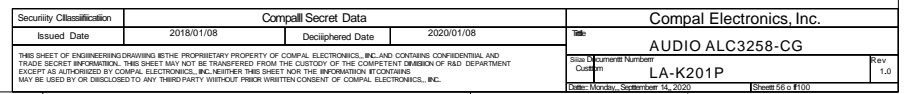


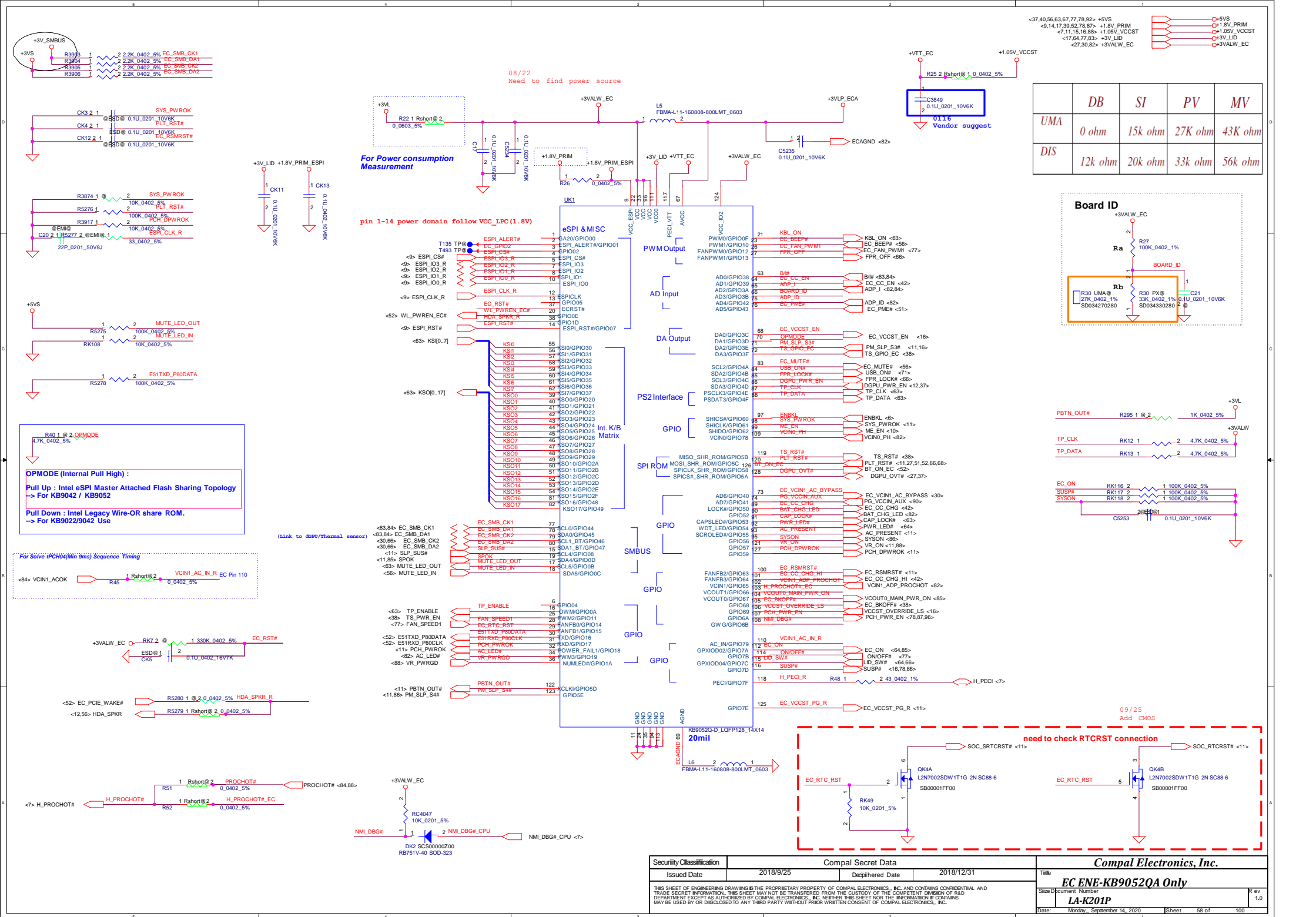
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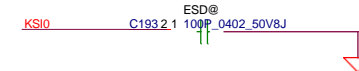
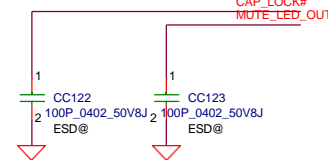
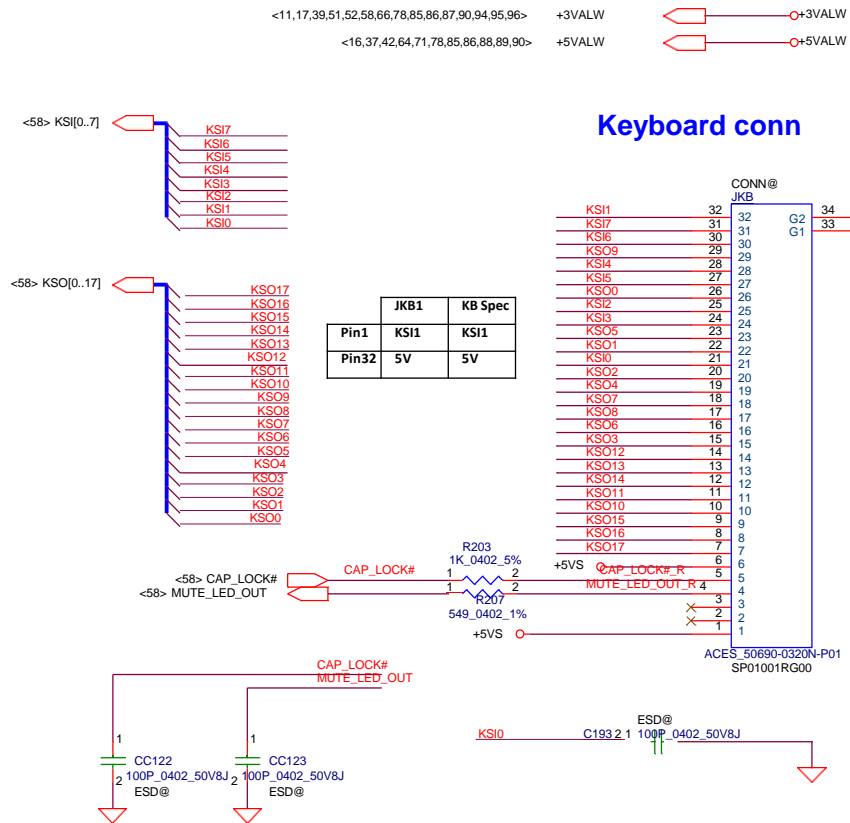
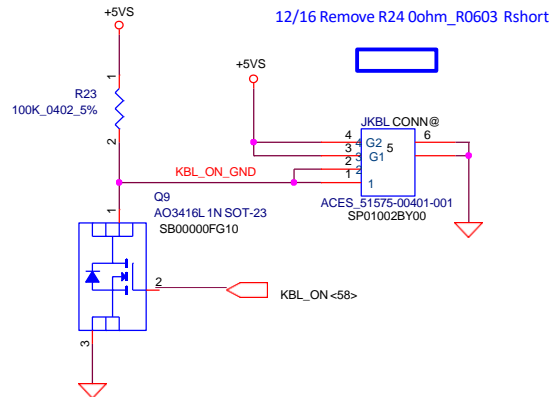
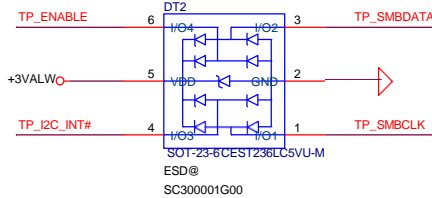
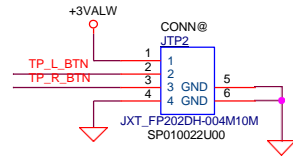
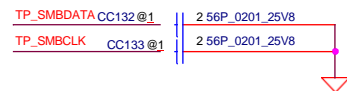
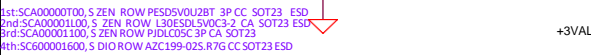
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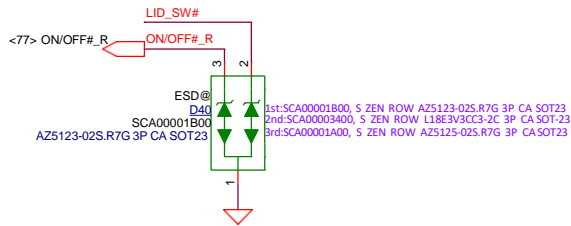
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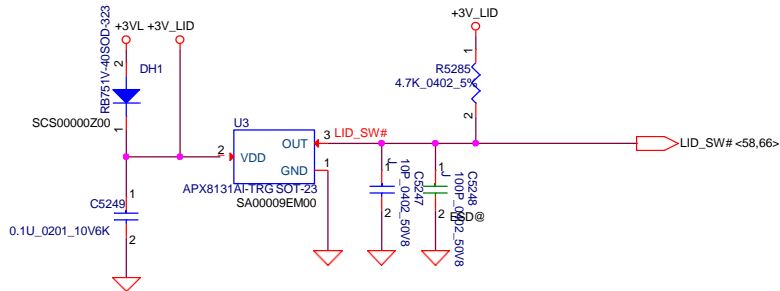
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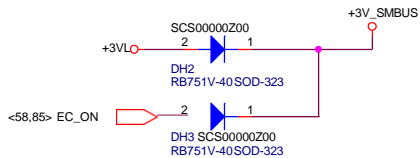
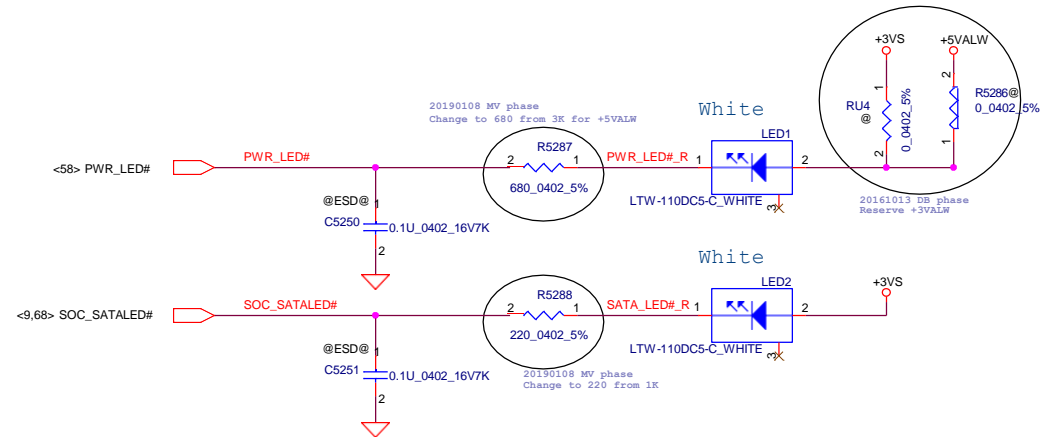
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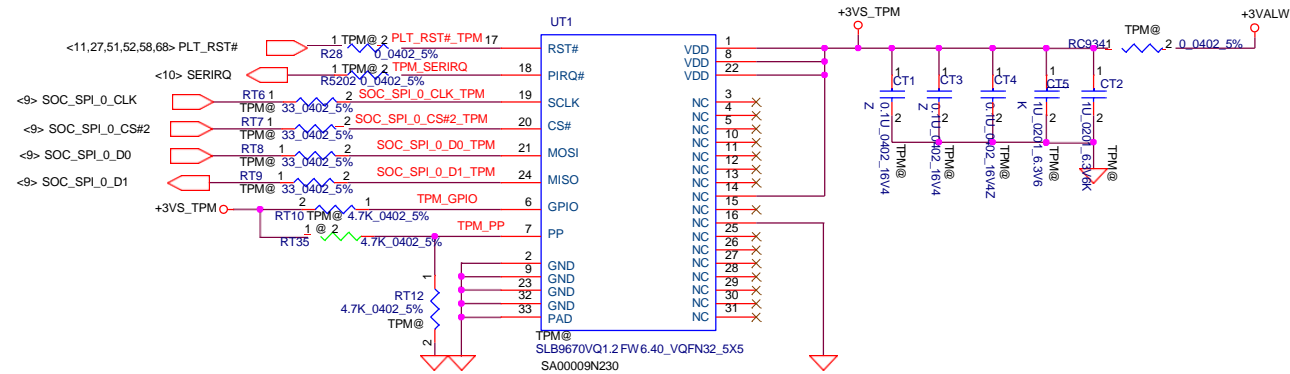


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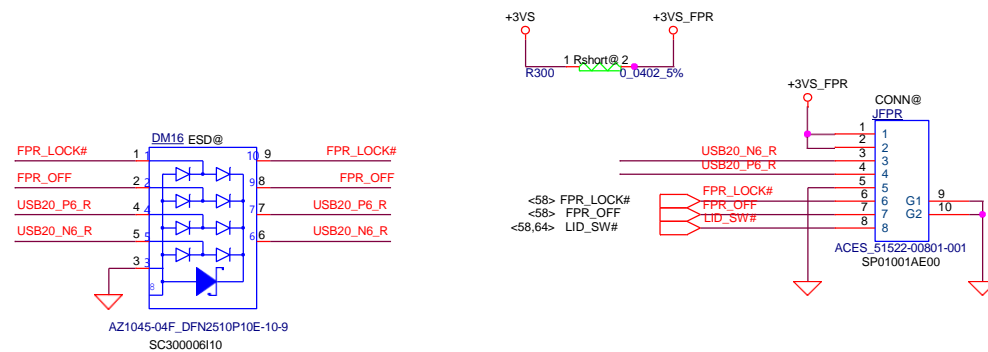


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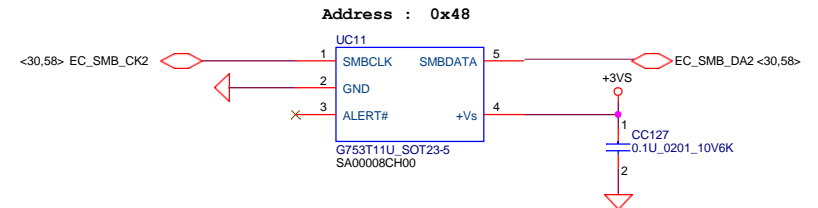
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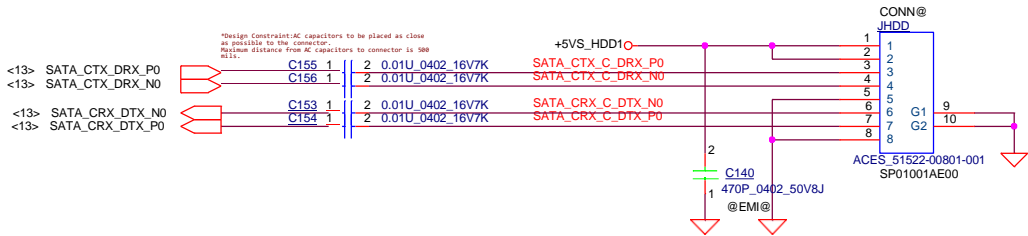
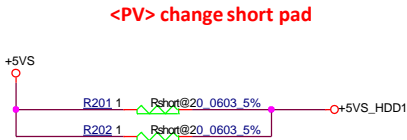


CPU THERMAL SENSOR

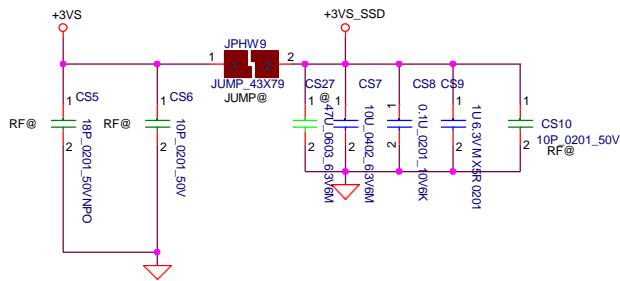


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2.5" SATA HDD



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Date: Monday, September 14, 2020				Sheet 67 of 100	



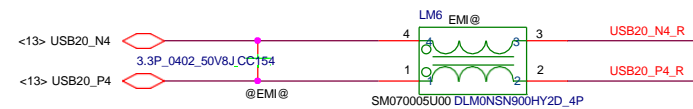
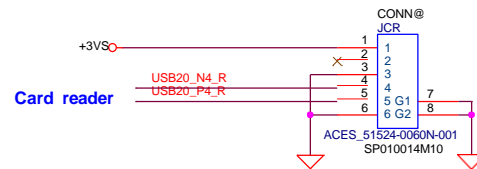
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+3VS

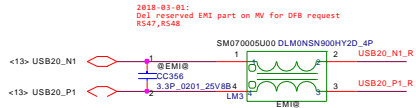
Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCIe Link Details	PCIe Controller #1	PCIe Controller #2	PCIe Controller #3
Line 00 Line 2	1	2	3
Line 01 Line 3	4	5	6
Line 02 Line 4	7	8	9
Line 03 Line 5	10	11	12
Line 04 Line 6	13	14	15
Line 05 Line 7	16	17	18
Line 06 Line 8	19	20	21
Line 07 Line 9	22	23	24
Line 08 Line 10	25	26	27
Line 09 Line 11	28	29	30
Line 10 Line 12	31	32	33
Line 11 Line 13	34	35	36
Line 12 Line 14	37	38	39
Line 13 Line 15	40	41	42
Line 14 Line 16	43	44	45
Line 15 Line 17	46	47	48
Line 16 Line 18	49	50	51
Line 17 Line 19	52	53	54
Line 18 Line 20	55	56	57
Line 19 Line 21	58	59	60
Line 20 Line 22	61	62	63
Line 21 Line 23	64	65	66
Line 22 Line 24	67	68	69
Line 23 Line 25	70	71	72
Line 24 Line 26	73	74	75
Line 25 Line 27	76	77	78
Line 26 Line 28	79	80	81
Line 27 Line 29	82	83	84
Line 28 Line 30	85	86	87
Line 29 Line 31	88	89	90
Line 30 Line 32	91	92	93
Line 31 Line 33	94	95	96
Line 32 Line 34	97	98	99
Line 33 Line 35	100	101	102
Line 34 Line 36	103	104	105
Line 35 Line 37	106	107	108
Line 36 Line 38	109	110	111
Line 37 Line 39	112	113	114
Line 38 Line 40	115	116	117
Line 39 Line 41	118	119	120
Line 40 Line 42	121	122	123
Line 41 Line 43	124	125	126
Line 42 Line 44	127	128	129
Line 43 Line 45	130	131	132
Line 44 Line 46	133	134	135
Line 45 Line 47	136	137	138
Line 46 Line 48	139	140	141
Line 47 Line 49	142	143	144
Line 48 Line 50	145	146	147
Line 49 Line 51	148	149	150
Line 50 Line 52	151	152	153
Line 51 Line 53	154	155	156
Line 52 Line 54	157	158	159
Line 53 Line 55	160	161	162
Line 54 Line 56	163	164	165
Line 55 Line 57	166	167	168
Line 56 Line 58	169	170	171
Line 57 Line 59	172	173	174
Line 58 Line 60	175	176	177
Line 59 Line 61	178	179	180
Line 60 Line 62	181	182	183
Line 61 Line 63	184	185	186
Line 62 Line 64	187	188	189
Line 63 Line 65	190	191	192
Line 64 Line 66	193	194	195
Line 65 Line 67	196	197	198
Line 66 Line 68	199	200	201
Line 67 Line 69	202	203	204
Line 68 Line 70	205	206	207
Line 69 Line 71	208	209	210
Line 70 Line 72	211	212	213
Line 71 Line 73	214	215	216
Line 72 Line 74	217	218	219
Line 73 Line 75	220	221	222
Line 74 Line 76	223	224	225
Line 75 Line 77	226	227	228
Line 76 Line 78	229	230	231
Line 77 Line 79	232	233	234
Line 78 Line 80	235	236	237
Line 79 Line 81	238	239	240
Line 80 Line 82	241	242	243
Line 81 Line 83	244	245	246
Line 82 Line 84	247	248	249
Line 83 Line 85	250	251	252
Line 84 Line 86	253	254	255
Line 85 Line 87	256	257	258
Line 86 Line 88	259	260	261
Line 87 Line 89	262	263	264
Line 88 Line 90	265	266	267
Line 89 Line 91	268	269	270
Line 90 Line 92	271	272	273
Line 91 Line 93	274	275	276
Line 92 Line 94	277	278	279
Line 93 Line 95	280	281	282
Line 94 Line 96	283	284	285
Line 95 Line 97	286	287	288
Line 96 Line 98	289	290	291
Line 97 Line 99	292	293	294
Line 98 Line 100	295	296	297
Line 99 Line 101	298	299	300
Line 100 Line 102	301	302	303
Line 101 Line 103	304	305	306
Line 102 Line 104	307	308	309
Line 103 Line 105	310	311	312
Line 104 Line 106	313	314	315
Line 105 Line 107	316	317	318
Line 106 Line 108	319	320	321
Line 107 Line 109	322	323	324
Line 108 Line 110	325	326	327
Line 109 Line 111	328	329	330
Line 110 Line 112	331	332	333
Line 111 Line 113	334	335	336
Line 112 Line 114	337	338	339
Line 113 Line 115	340	341	342
Line 114 Line 116	343	344	345
Line 115 Line 117	346	347	348
Line 116 Line 118	349	350	351
Line 117 Line 119	352	353	354
Line 118 Line 120	355	356	357
Line 119 Line 121	358	359	360
Line 120 Line 122	361	362	363
Line 121 Line 123	364	365	366
Line 122 Line 124	367	368	369
Line 123 Line 125	370	371	372
Line 124 Line 126	373	374	375
Line 125 Line 127	376	377	378
Line 126 Line 128	379	380	381
Line 127 Line 129	382	383	384
Line 128 Line 130	385	386	387
Line 129 Line 131	388	389	390
Line 130 Line 132	391	392	393
Line 131 Line 133	394	395	396
Line 132 Line 134	397	398	399
Line 133 Line 135	400	401	402
Line 134 Line 136	403	404	405
Line 135 Line 137	406	407	408
Line 136 Line 138	409	410	411
Line 137 Line 139	412	413	414
Line 138 Line 140	415	416	417
Line 139 Line 141	418	419	420
Line 140 Line 142	421	422	423
Line 141 Line 143	424	425	426
Line 142 Line 144	427	428	429
Line 143 Line 145	430	431	432
Line 144 Line 146	433	434	435
Line 145 Line 147	436	437	438
Line 146 Line 148	439	440	441
Line 147 Line 149	442	443	444
Line 148 Line 150	445	446	447
Line 149 Line 151	448	449	450
Line 150 Line 152	451	452	453
Line 151 Line 153	454	455	456
Line 152 Line 154	457	458	459
Line 153 Line 155	460	461	462
Line 154 Line 156	463	464	465
Line 155 Line 157	466	467	468
Line 156 Line 158	469	470	471
Line 157 Line 159	472	473	474
Line 158 Line 160	475	476	477
Line 159 Line 161	478	479	480
Line 160 Line 162	481	482	483
Line 161 Line 163	484	485	486
Line 162 Line 164	487	488	489
Line 163 Line 165	490	491	492
Line 164 Line 166	493	494	495
Line 165 Line 167	496	497	498
Line 166 Line 168	499	500	501
Line 167 Line 169	502	503	504
Line 168 Line 170	505	506	507
Line 169 Line 171	508	509	510
Line 170 Line 172	511	512	513
Line 171 Line 173	514	515	516
Line 172 Line 174	517	518	519
Line 173 Line 175	520	521	522
Line 174 Line 176	523	524	525
Line 175 Line 177	526	527	528
Line 176 Line 178	529	530	531
Line 177 Line 179	532	533	534
Line 178 Line 180	535	536	537
Line 179 Line 181	538	539	540
Line 180 Line 182	541	542	543
Line 181 Line 183	544	545	546
Line 182 Line 184	547	548	549
Line 183 Line 185	550	551	552
Line 184 Line 186	553	554	555
Line 185 Line 187	556	557	558
Line 186 Line 188	559	560	561
Line 187 Line 189	562	563	564
Line 188 Line 190	565	566	567
Line 189 Line 191	568	569	570
Line 190 Line 192	571	572	573
Line 191 Line 193	574	575	576
Line 192 Line 194	577	578	579
Line 193 Line 195	580	581	582
Line 194 Line 196	583	584	585
Line 195 Line 197	586	587	588
Line 196 Line 198	589	590	591
Line 197 Line 199	592	593	594
Line 198 Line 200	595	596	597
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Line 201 Line 203	604	605	606
Line 202 Line 204	607	608	609
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Line 204 Line 206	613	614	615
Line 205 Line 207	616	617	618
Line 206 Line 208	619	620	621
Line 207 Line 209	622	623	624
Line 208 Line 210	625	626	627
Line 209 Line 211	628	629	630
Line 210 Line 212	631	632	633
Line 211 Line 213	634	635	636
Line 212 Line 214	637	638	639
Line 213 Line 215	640	641	642
Line 214 Line 216	643	644	645
Line 215 Line 217	646	647	648
Line 216 Line 218	649	650	651
Line 217 Line 219	652	653	654
Line 218 Line 220	655	656	657
Line 219 Line 221	658	659	660
Line 220 Line 222	661	662	663
Line 221 Line 223	664	665	666
Line 222 Line 224	667	668	669
Line 223 Line 225	670	671	672
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Line 228 Line 230	685	686	687
Line 229 Line 231	688	689	690
Line 230 Line 232	691	692	693
Line 231 Line 233	694	695	696
Line 232 Line 234	697	698	699
Line 233 Line 235	700	701	702
Line 234 Line 236	703	704	705
Line 235 Line 237	706	707	708
Line 236 Line 238	709	710	711
Line 237 Line 239	712	713	714
Line 238 Line 240	715	716	717
Line 239 Line 241	718	719	720
Line 240 Line 242	721	722	723
Line 241 Line 243	724	725	726
Line 242 Line 244	727	728	729
Line 243 Line 245	730	731	732
Line 244 Line 246	733	734	735
Line 245 Line 247	736	737	738
Line 246 Line 248	739	740	741
Line 247 Line 249	742	743	744
Line 248 Line 250	745	746	747
Line 249 Line 251	748	749	750
Line 250 Line 252	751	752	753
Line 251 Line 253	754	755	756
Line 252 Line 254	757	758	759
Line 253 Line 255	760	761	762
Line 254 Line 256	763	764	765
Line 255 Line 257	766	767	768
Line 256 Line 258	769	770	771
Line 257 Line 259	772	773	774
Line 258 Line 260	775	776	777
Line 259 Line 261	778	779	780
Line 260 Line 262	781	782	783
Line 261 Line 263	784	785	786
Line 262 Line 264	787	788	789
Line 26			

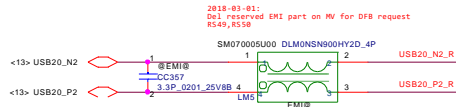
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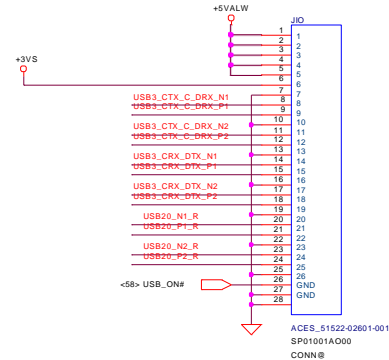
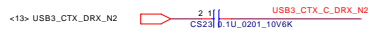
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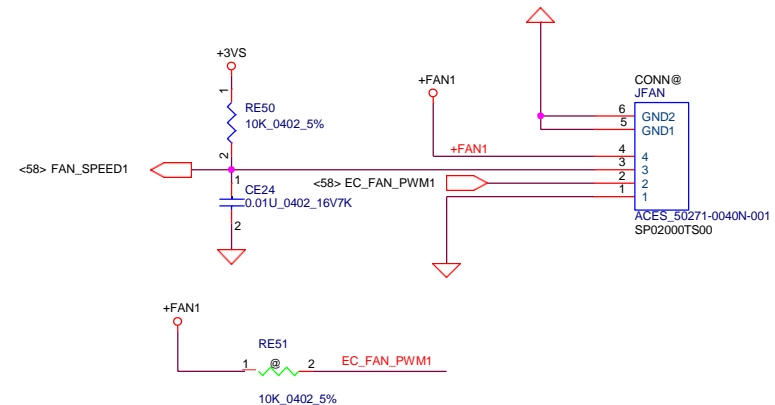
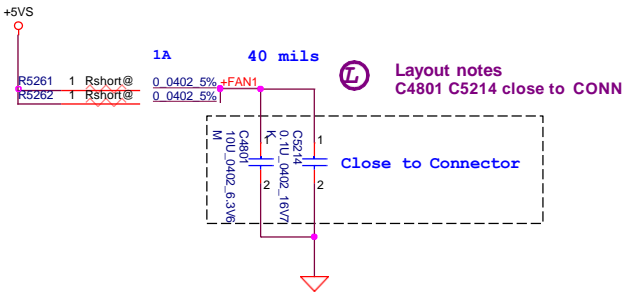
USB 2.0/3.0
MURATA DLM0 NS900 HY 2D (MURATA)
DO1 reserved EMI part on MV for DFB request
R547,R548



USB 2.0/3.0
MURATA DLM0 NS900 HY 2D (MURATA)
DO1 reserved EMI part on MV for DFB request
R549,R550

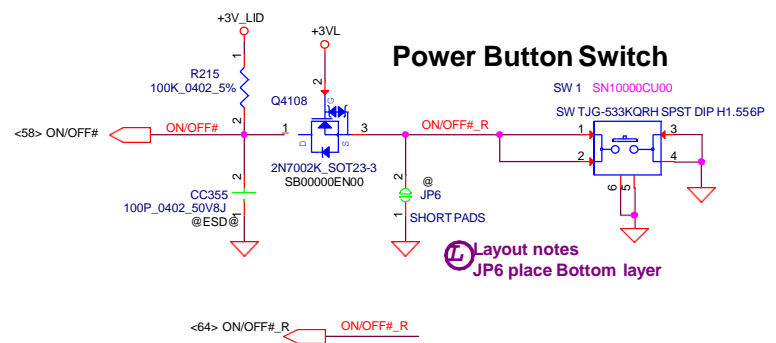
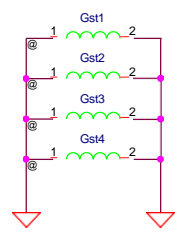
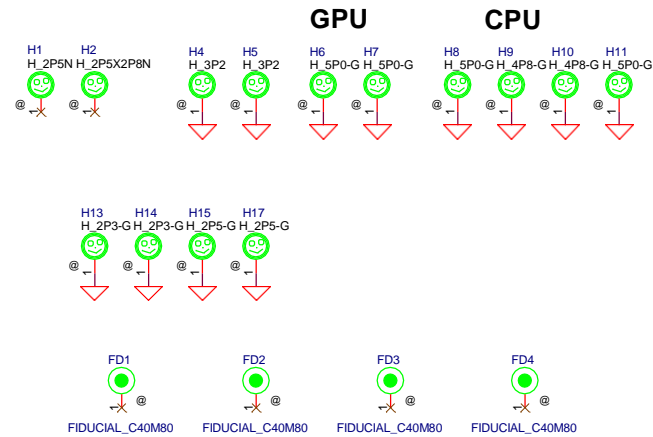


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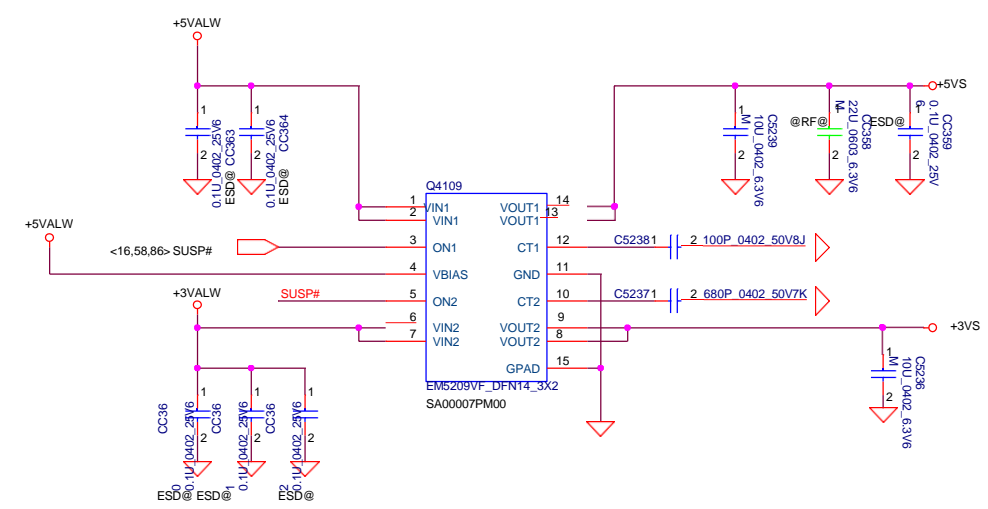
Screw Hole

EMI Gasket

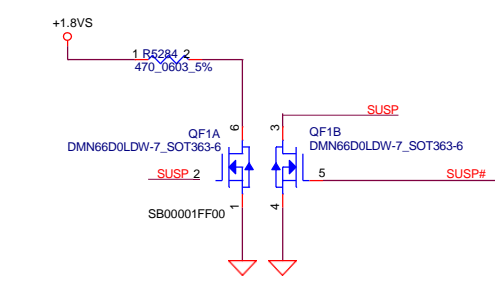
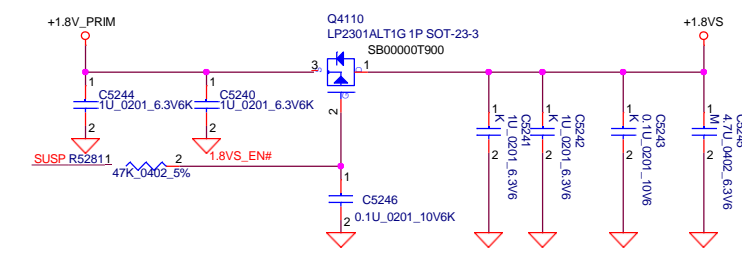


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Date: Monday, September 14, 2020				Sheet 77 of 100	

+3VS <8,9,11,12,13,23,24,31,37,38,39,40,51,56,58,64,66,68,70,71,77,88,92,94,95>
+5VS <37,40,56,58,63,67,77,92>

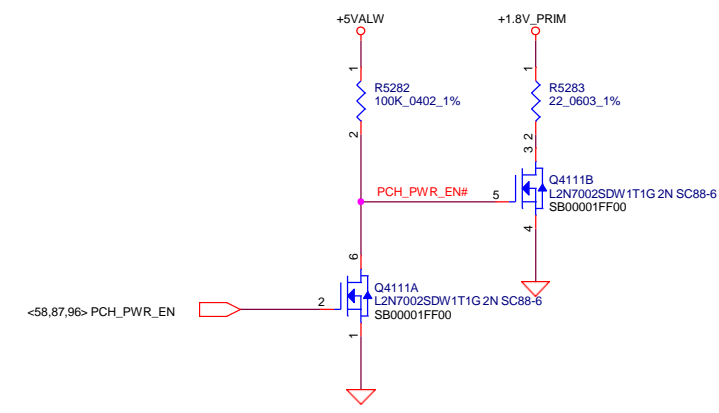


+1.8V_PRIM TO +1.8VS
I (Max) : 0.2 A (Codec)
RDS (max) : 150 mohm
V drop : 0.03V

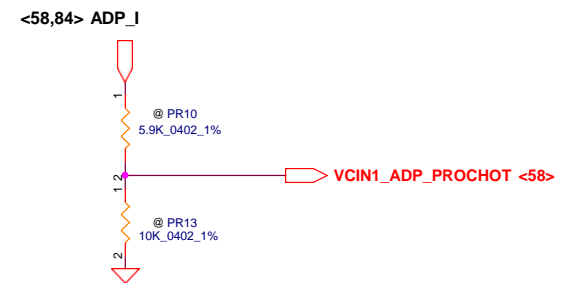
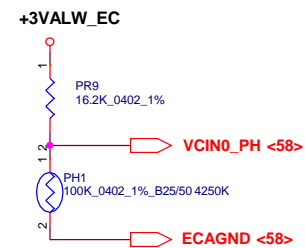
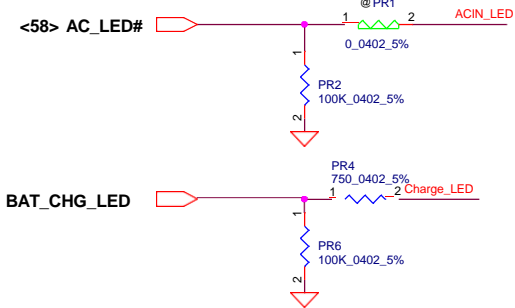
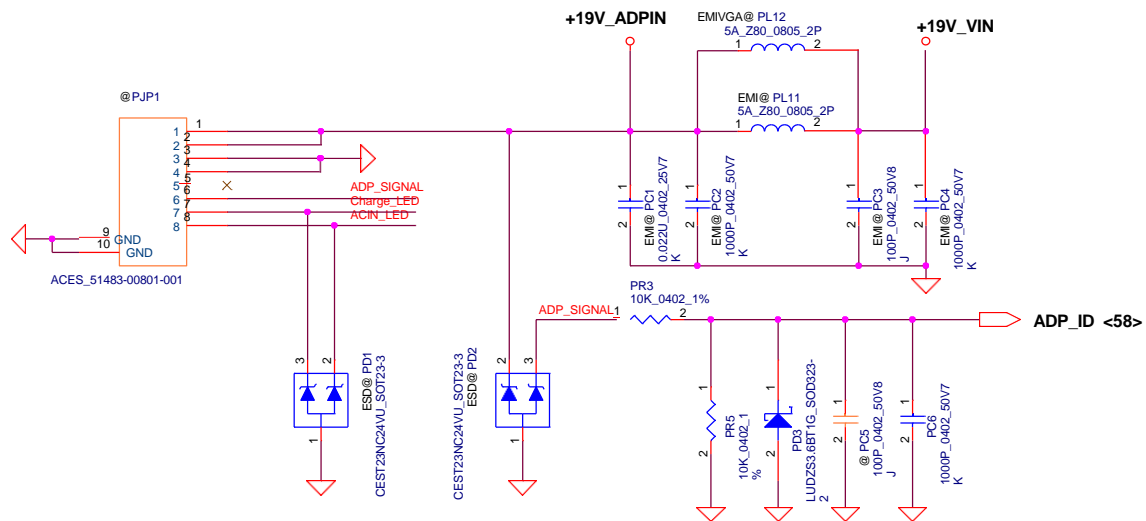


Add +1.8VS power down

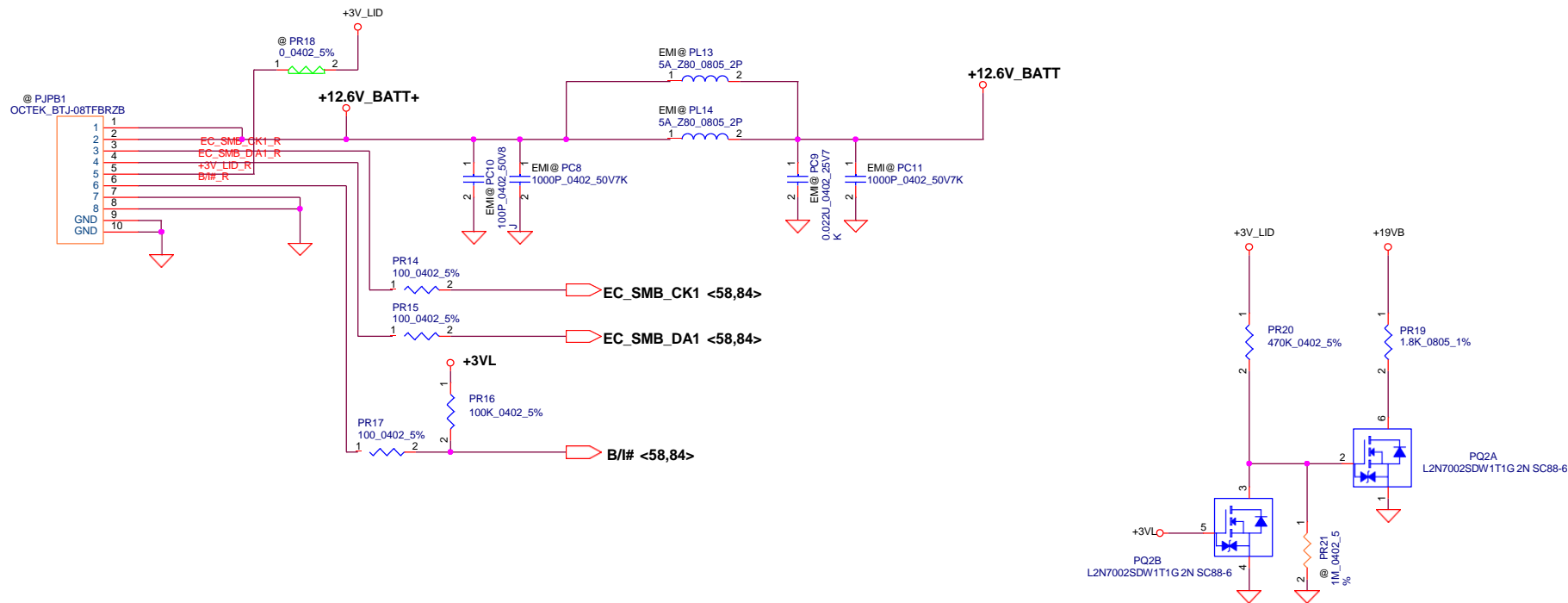
For +1.8V_PRIM Discharge



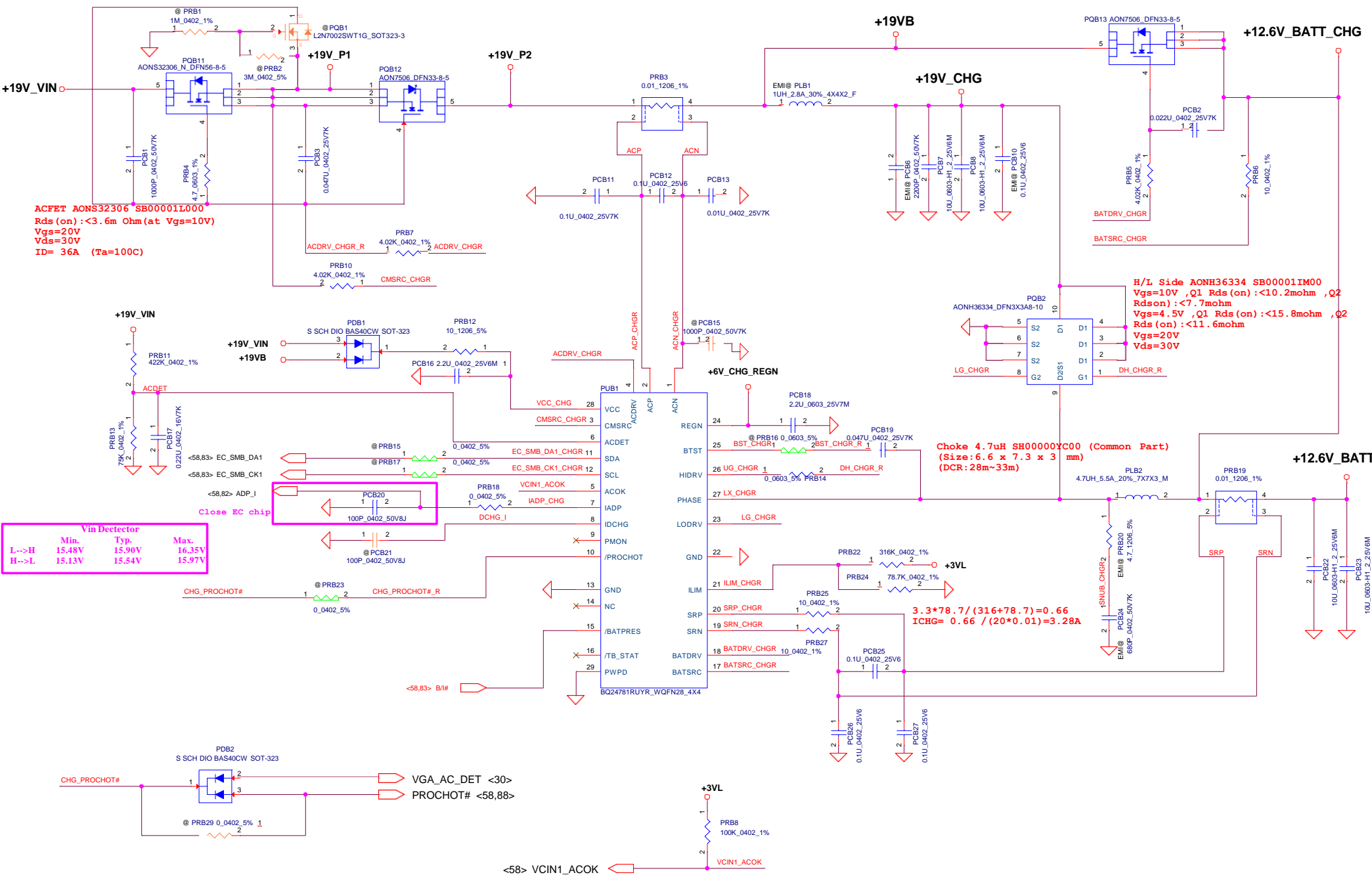
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								Date:		Monday, September 14, 2020		Sheet 78 of 100	
								C		D		E	



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				Date	Monday, September 14, 2020
				Sheet	83 of 100
				Rev	v0.3



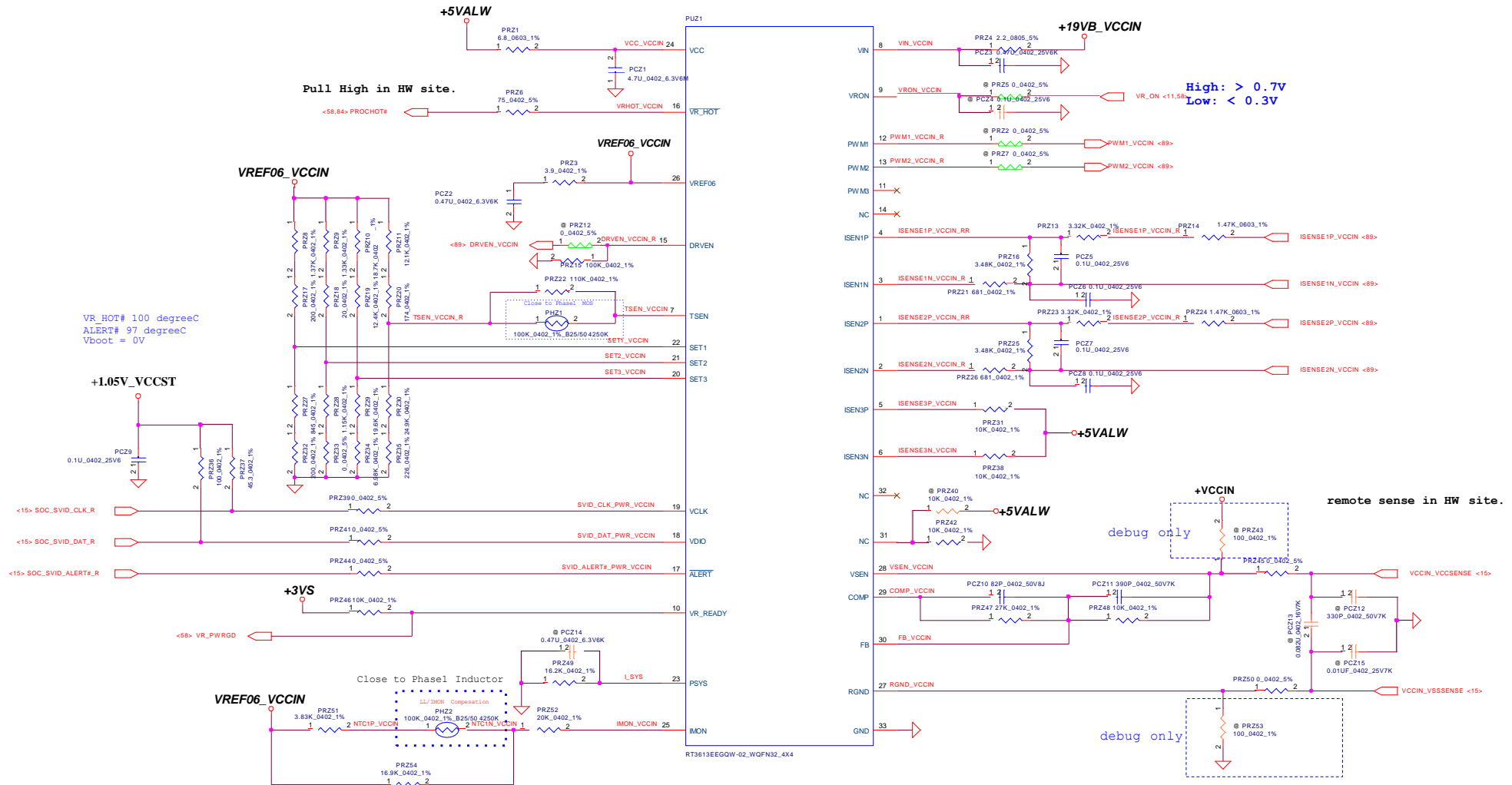
ACFET AONS32306 SB00001I000
Rds(on) : <3.6m Ohm (at Vgs=10V)
Vgs=20V
Vds=30V
ID= 36A (Ta=100C)

Vin Dectector			
	Min.	Typ.	Max.
L-->H	15.48V	15.90V	16.35V
H-->L	15.13V	15.54V	15.97V

When Charegr chg_PROCHOT#R low, the cpu(PROCHOT#)
and gpu(VGA_AC_DET) will be low.

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Date: Monday, September 14, 2020				Sheet 84 of 100

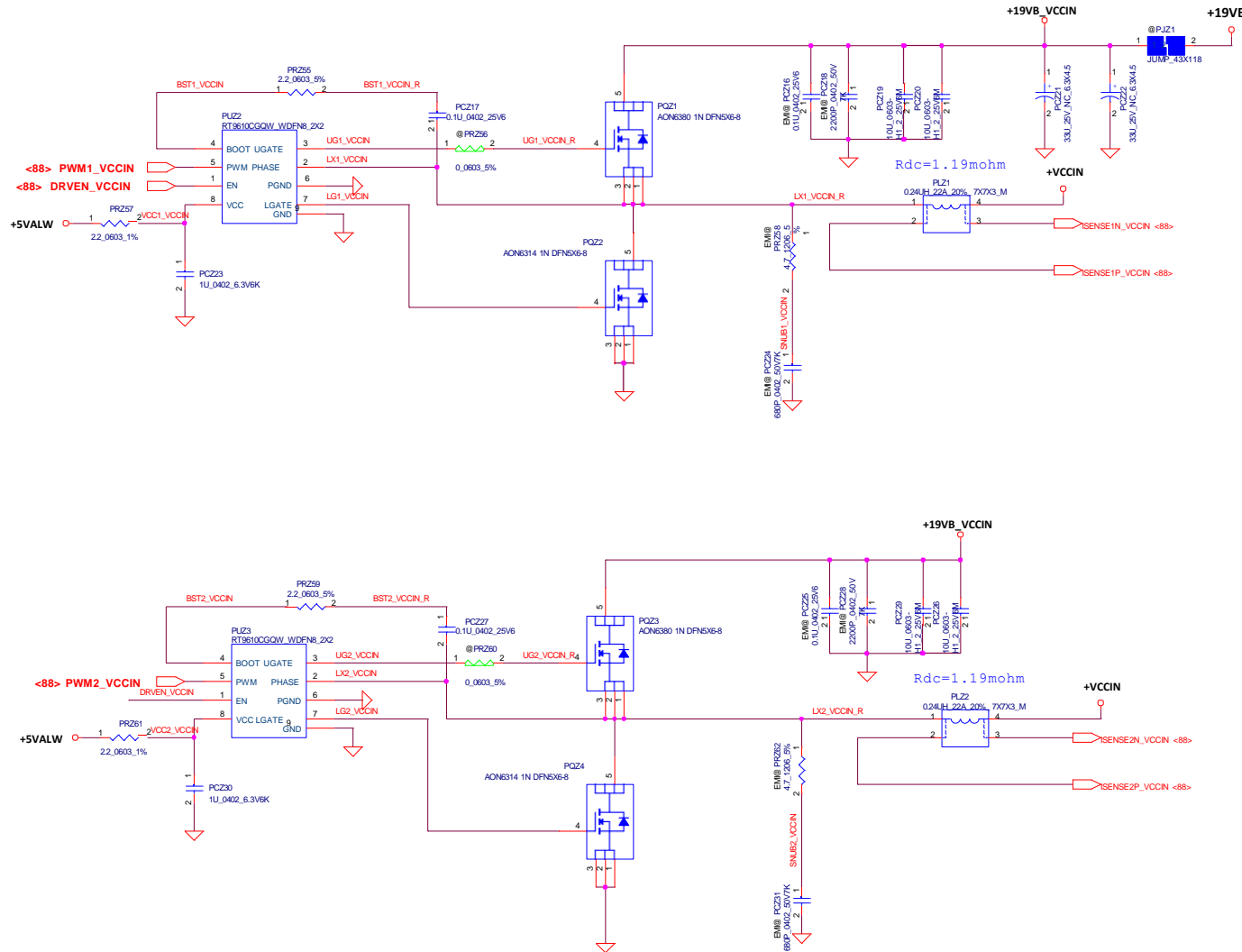
RT3613EEGQW-02 is not MP part



31 pin is a function to fix decay down slew rate to reduce acoustic noise.
High(5V): enable
Low:(0V): disable
this pin can dynamic change state.

AON6380
R DS(ON) (at V GS =10V) < 6.8mohm
R DS(ON) (at V GS =4.5V) < 10.5mohm

AON6314
R DS(ON) (at V GS =10V) < 2.8mohm
R DS(ON) (at V GS =4.5V) < 3.5mohm



For 2 phase:
OCP=74.1A
ICCMAX=47A
TDC=30A
DC_LL=2mohm
AC_LL=4.4mohm

AON6380
R DS (ON) (at V GS =10V) < 6.8mohm
R DS (ON) (at V GS =4.5V) < 10.5mohm
AON6314
R DS (ON) (at V GS =10V) < 2.8mohm
R DS (ON) (at V GS =4.5V) < 3.5mohm

OCP is Lowside MOSFET Rdsn sense

226K x1.2
255K x1.4

+5VALW

High > 1V
Low < 0.4V

+3VALW

+5VALW

5V: 800KHz
Float: 600KHz
GND: 400KHz

VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

+19VB_AUX

+VCCIN_AUX

+VCCIN_AUX

+19VB_AUX

+19VB

ICCMAX=32A
TDC=14A
AC_LL: <1MHz 4.9 1-40MHz 8

+VCCIN_AUX

330u*1
22u_0603*12

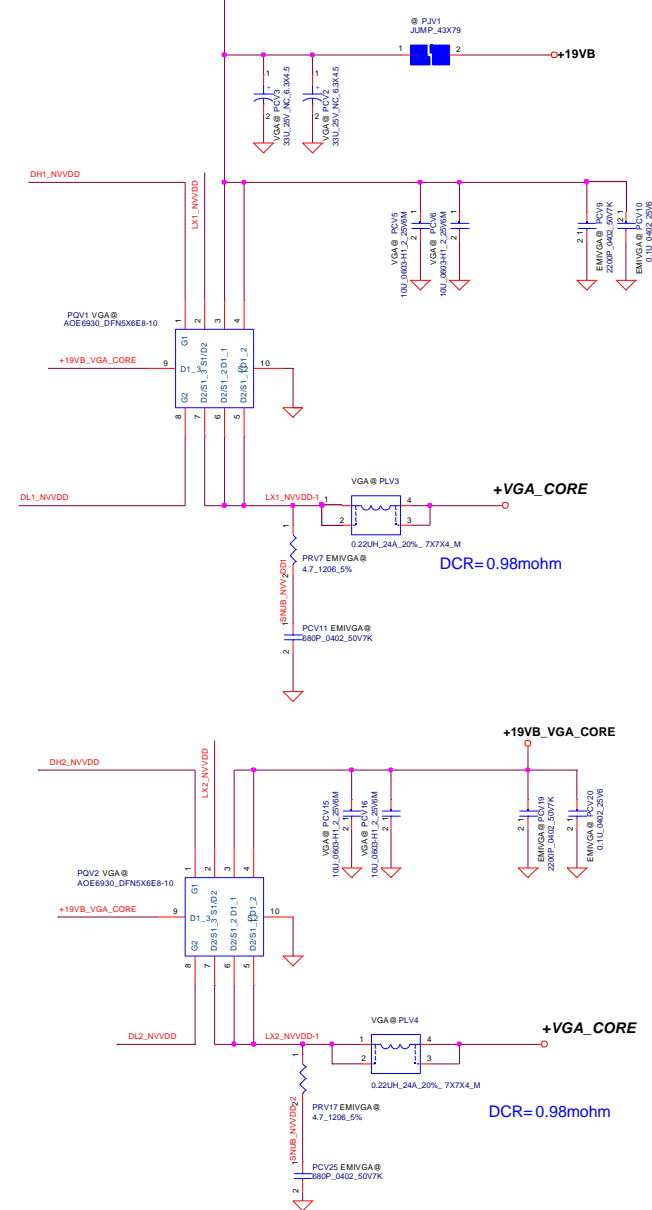
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				Version	Rev A0.3

PWM-VID Spec and component Values

PWM-VID Spec	
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V
Voltage step	6.25mV
N of Voltage level	160
Rrefadj	PRV10 6.19K
Rref1	PRV8 20.5K
Rboot	PRV9 4.32K
Rref2=PRV8+PRV11	PRV11 16.5K
C	PRV13 0.309K
	PCV13 4.7nf

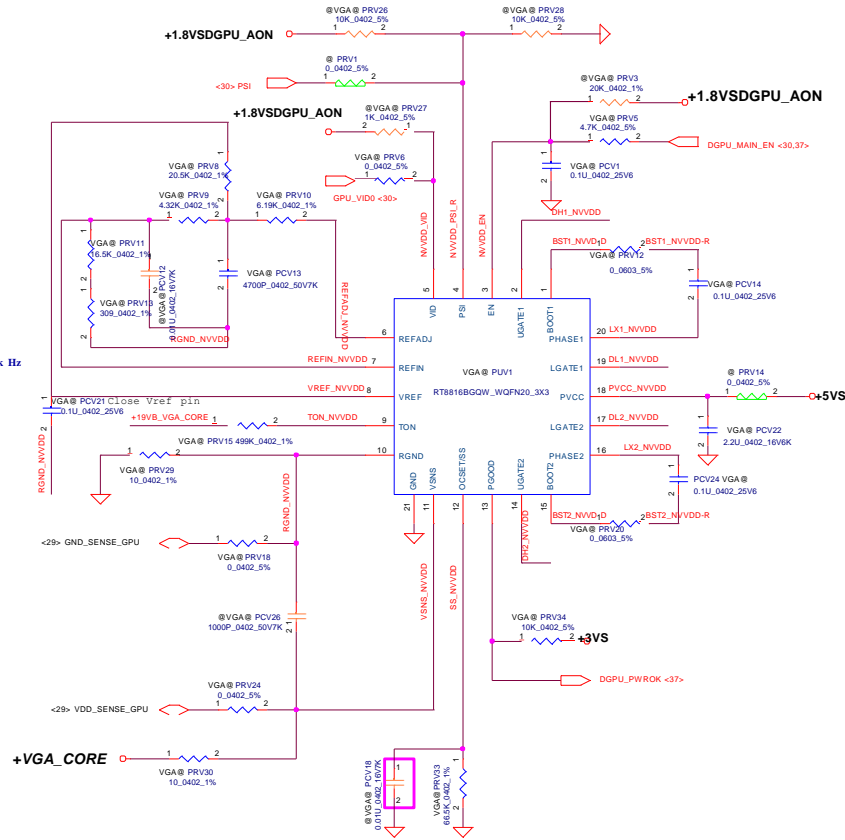
VGA Chip	N17S-G5	VGA Chip	N18S-G5
OpenVReg Configurations		OpenVReg Configurations	
Rated TDP Power at Tj=102C	25W	Rated TDP Power at Tj=102C	25W
EDP-Continuous at Tj=102C	35A	EDP-Continuous at Tj=102C	35A
EDP-Peak at Tj=102C	70A	EDP-Peak at Tj=102C	75A
Istep max (Evaluation)	A	Istep max (Evaluation)	A
OCp Setting Current	92A	OCp Setting Current	92A
Rocset	66.5K	Rocset	66.5K
Recommendation	2phase	Recommendation	2phase

+19VB_VGA_CORE



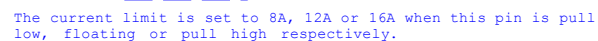
VGAN17@
TDC = 35A
Ipeak = 78A
OCP = 92A(valley)

VGAN18@
TDC = 30A
Ipeak = 75A
OCP = 92A(valley)



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					2019OPP TGL
					Monday, September 14, 2020 Sheet 52 of 100

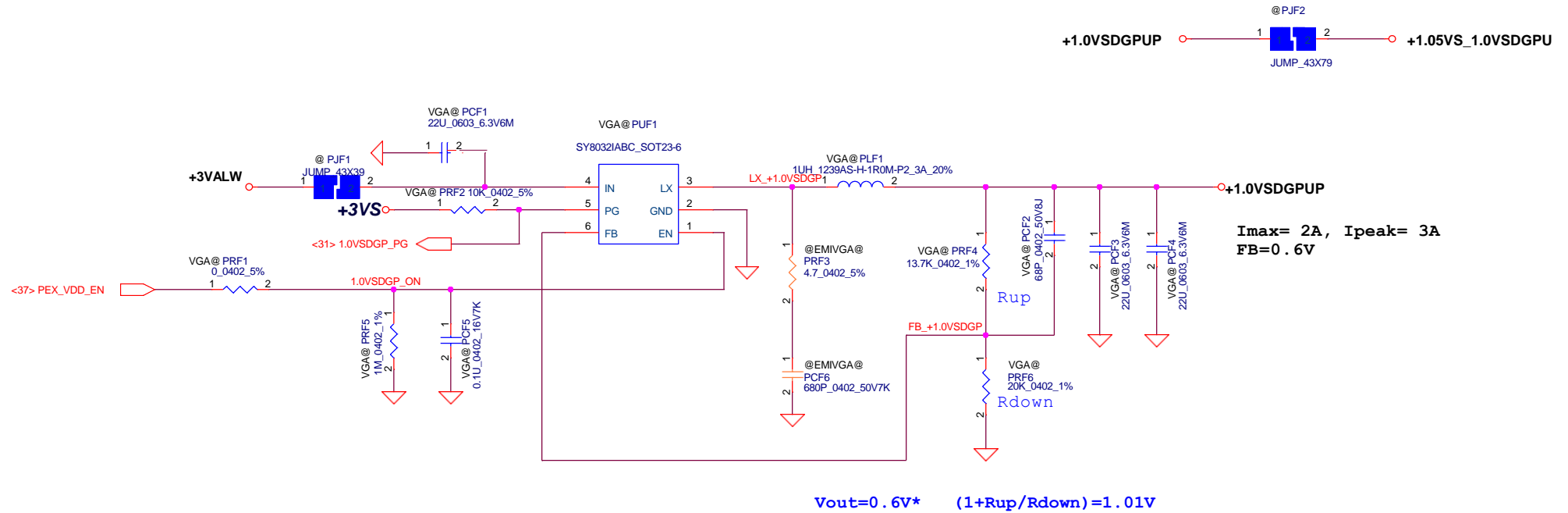
VGAN18@
TDC = 7A
Ipeak = 8A



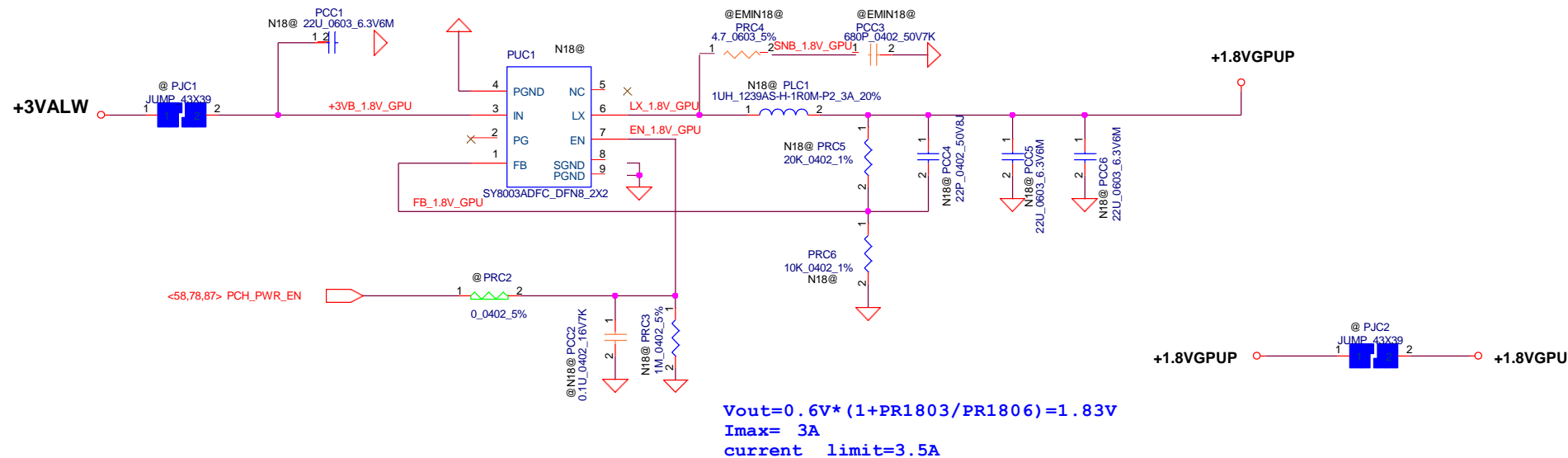
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/09/01	Deciphered Date	2019/09/01	Title +I.35VS_VRAM	
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				2019OPP TGL	
Date: Monday, September 14, 2020				Sheet	94 of 100

VGA N17@
TDC = 0.3A
Ipeak = 0.4A

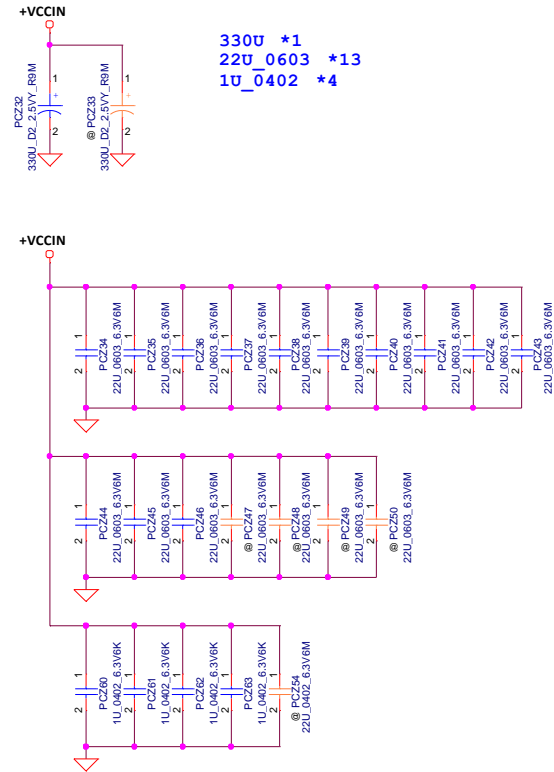
VGA N18@
TDC = 1.6A
Ipeak = 1.9A



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Date:	Monday, September 14, 2020	Sheet	95	of	100	

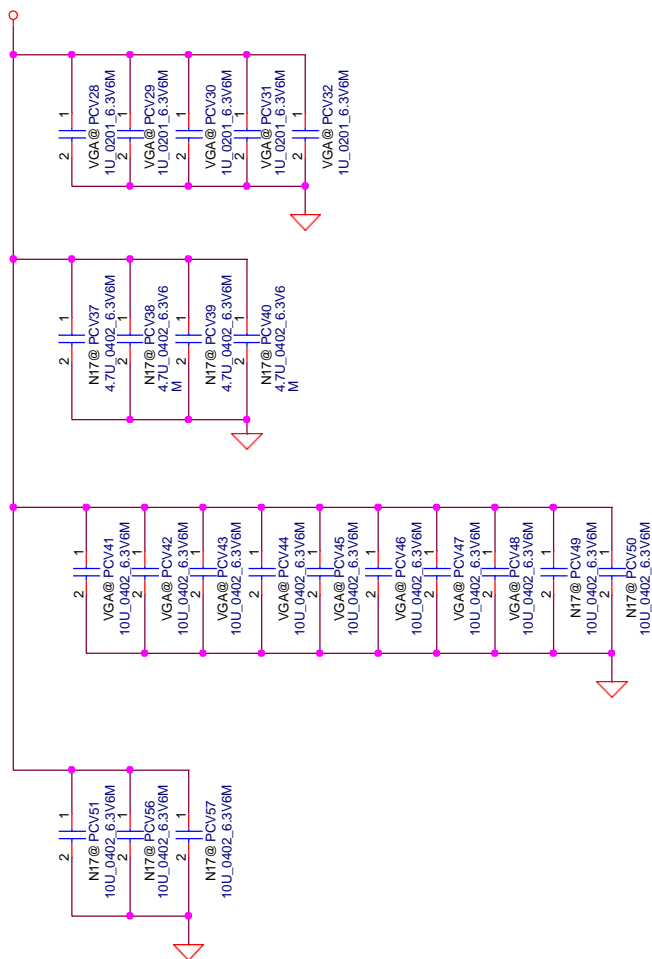


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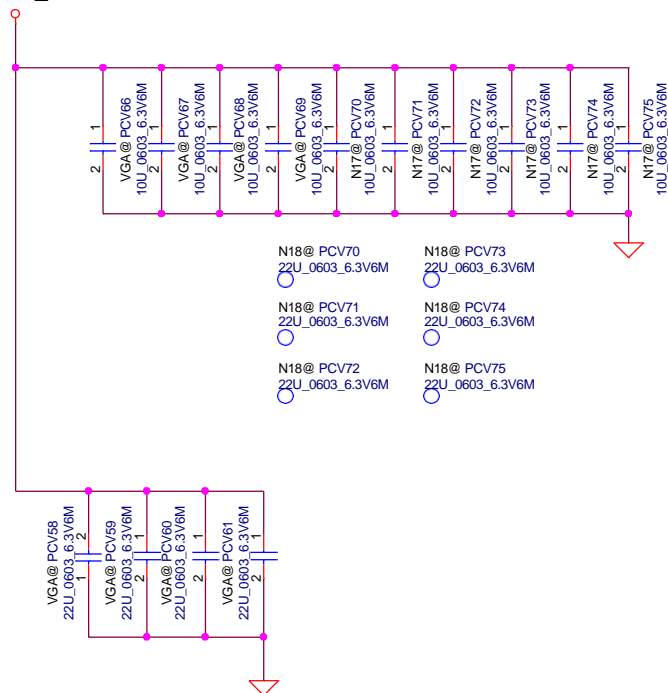


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				Size Document Number	Rev
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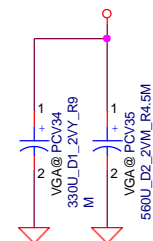
+VGA_CORE



+VGA_CORE



+VGA_CORE



N17@		N18@	
1uF(0201)	x 5	1uF(0201)	x 5
4.7uF(0402)	x 4	4.7uF(0402)	x 0
10uF(0402)	x 13	10uF(0402)	x 8
10uF(0603)	x 10	10uF(0603)	x 4
22uF(0603)	x 4	22uF(0603)	x 10
330uF x 1		330uF x 1	
560uF x 1		560uF x 1	

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Version change list
(P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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				Custom	
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